GigaDevice Semiconductor Inc.

Guidelines for Hardware Development of GD32F5xx

Application Notes
AN182

Version 1.1

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1. Foreword

This document is specially provided for developers of the general-purpose 32-bit GD32F5xx MCU based on the Arm® Cortex®-M33 architecture. It provides a general introduction to the hardware development of GD32F5xx, such as power supply, reset, clock, setting of boot mode, and download debug. The purpose of the Application Notes is to enable developers to quickly get started with GD32F5xx, quickly develop and use the product hardware, and save time for studying the manual, thus accelerating the product development progress.

The Application Notes is described in eight parts:

1. Power supply: It mainly introduces the design of the power management, power supply, and reset functions of GD32F5xx.
2. Clock: It mainly introduces the design of the high and low speed clock functions of GD32F5xx.
3. Boot configuration: It mainly introduces the BOOT configuration and design of GD32F5xx.
4. Typical peripheral module: It mainly introduces the hardware design of the main functional modules of GD32F5xx.
5. Download debug circuit: It mainly introduces the typical download debug circuits recommended for GD32F5xx.
6. Reference circuit and PCB layout design: It mainly introduces the precautions for hardware circuit design and PCB layout design of GD32F5xx series.
7. Steel mesh and soldering: It mainly introduces the selection and usage method of the steel mesh and the reflow soldering temperature curves.
8. Package description: It mainly introduces the types and names of packages included in GD32F5xx.

This document also introduces the minimum system hardware resources used in GD32F5xx application development.

Table 1-1. Applicable product

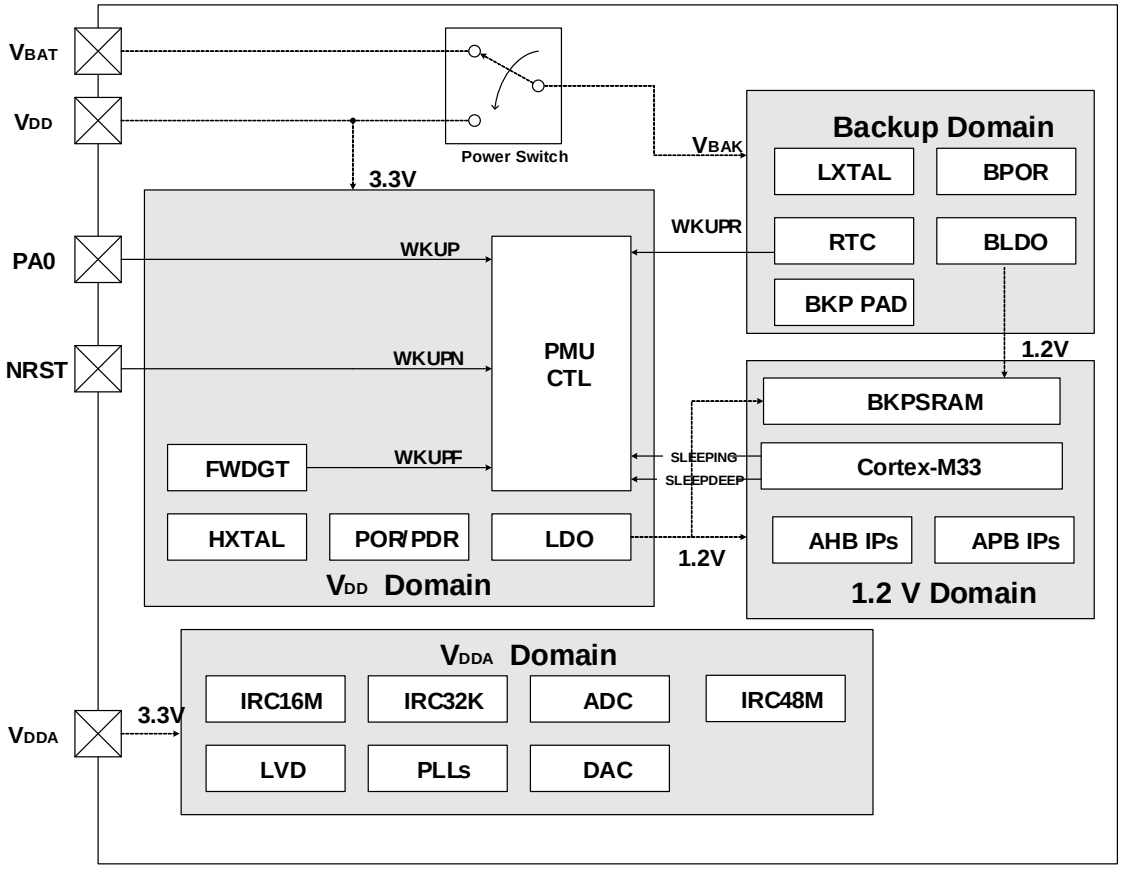
Type	Model
MCU	GD32F527xx Series

2. Hardware design

2.1. Power supply

The operating voltage of V_{DD} / V_{DDA} domain of GD32F5xx ranges from 1.71 V to 3.6 V. As shown in ***Figure 2-1. Overview of power domains of GD32F5xx***, GD32F5xx MCU has three power domains, including V_{DD}/V_{DDA} domain, 1.2 V domain, and backup domain. V_{DD}/V_{DDA} domain is directly powered by the power supply, and an LDO is embedded in the V_{DD}/V_{DDA} domain to power the 1.2 V domain. In the backup domain, there is a power switch. When the VDD power supply is turned off, the power switch can switch the power supply of the backup domain to the VBAT pin (battery). At this time, the backup domain is powered by the VBAT pin (battery). When the backup domain is only powered by V_{BAT} pin, the BLDO in the backup domain powers the backup SRAM of the 1.2 V domain under the condition that BLDOON in PMU_CS register is set, to ensure that the user data are not lost when V_{DD} is disconnected.

Figure 2-1. Overview of power domains of GD32F5xx



LVD：Low Voltage Detector
LDO：Voltage Regulator
BPOR：V_{BAK} Power On Reset
POR：Power On Reset
PDR：Power Down Reset
BLDO：Backup SRAM LDO Output 1.2 V
BKPSRAM: Backup SRAM

2.1.1. Backup domain

The supply voltage of backup domain ranges from 1.71 V to 3.6 V. The power switch in the backup domain selects V_{DD} or V_{BAT} (battery) as the power supply, and then V_{BAK} powers the backup domain. In order to ensure the contents of the register in the backup domain and normal operation of RTC, when V_{DD} is off, V_{BAT} pin can be powered by being connected to a battery or other backup power supply. If there are no battery-powered external applications, it is recommended to connect V_{BAT} pin to V_{DD} pin after being connected via a 100 nF capacitor to ground.

Precautions for V_{BAT} power supply:

In terms of power consumption of V_{BAT} pin, theoretically, when V_{DD} is powered on, the power switch in the backup domain is connected to V_{DD}, with no current passing through V_{BAT} pin. However, when ADC channel is used for V_{BAT} measurement in the main program, V_{BAT} will be divided by 4 due to MCU design and flow into ADC channel, thus causing extra power consumption (tens of uA) at V_{BAT} pin.

2.1.2. V_{DD}/V_{DDA} power domain

V_{DD}/V_{DDA} power domain includes two parts: V_{DD} domain and V_{DDA} domain. If V_{DDA} is not equal to V_{DD}, the voltage difference between them must not exceed 300 mV (V_{DDA} and V_{DD} inside the chip are connected through back-to-back diodes). To avoid noise, V_{DDA} can be connected to V_{DD} through an external filter circuit, and V_{SSA} can be connected to V_{SS} through a specific circuit (single-point grounding through 0 Ω resistors or magnetic beads, etc.).

In order to improve the conversion accuracy of ADC for better characteristics of the analog circuit, V_{DDA} can be separately powered. GD32F5xx contains V_{REFP} (1.8 V ≤ V_{REFP} ≤ V_{DDA}) for separate power supply to ADC.

GD32F5xx products contain V_{REFP} pin (for packages with at least 100 pins only), which can be powered by an external reference power supply or by being directly connected to V_{DDA} pin.

2.1.3. Power-saving modes

GD32F5xx provides three power-saving modes, namely sleep mode, deep sleep mode, and standby mode. Their comparison is listed in ***Table 2-1. Summary of power-saving modes***.

Table 2-1. Summary of power-saving modes

Mode	Sleep mode	Deep sleep mode	Standby mode
Description	Only the CPU clock is off.	1. Turn off all clocks in the 1.2 V domain. 2. Disable IRC16M, HXTAL, and PLL.	1. Power off the 1.2 V domain. 2. Disable IRC16M, HXTAL, and PLL.
LDO status	On (in normal power consumption and normal	On (in normal/low power consumption and normal/low	Off

Mode	Sleep mode	Deep sleep mode	Standby mode
	drive modes)	drive modes)	
Setting	SLEEPDEEP = 0	SLEEPDEEP = 1 STBMOD = 0	SLEEPDEEP = 1 STBMOD = 1, WURST = 1
Entry command	WFI or WFE	WFI or WFE	WFI or WFE
Wake-up	Wake up MCU from the sleep mode which was entered through WFI by any interrupt. Wake up MCU from the sleep mode which was entered through WFE by any event or interrupt in the case that the SEVONPEND bit is set to 1.	Wake up MCU from deep sleep mode which was entered through WFI by any interrupt. Wake up MCU from the deep sleep mode which was entered through WFE by any event from EXTI or interrupt in the case that the SEVONPEND bit is set to 1.	1. NRST pin 2. WKUP pin 3. FWDGT resetting 4. RTC
Delay in wake-up	None	IRC16M wake-up time The wake-up time shall be extended for LDO if it is in low power mode.	Power-on sequence

Note: In standby mode, all I/Os are in high impedance state, except NRST pin, PC13 and PI8 set to function as RTC, PC14 and PC15 used as pins of LXTAL crystal oscillator, and enabled WKUP pin. See ***Table 2-2. Power-saving modes of RTC*** for the power-saving modes of RTC.

Table 2-2. Power-saving modes of RTC

Mode	Whether to operate in such mode	Method for exiting from such mode
Sleep mode	Yes	RTC interrupt
Deep sleep mode	Operating when the clock source is LXTAL or IRC32K	RTC clock/intrusion/timestamp/wake-up event
Standby mode	Operating when the clock source is LXTAL or IRC32K	RTC clock/intrusion/timestamp/wake-up event

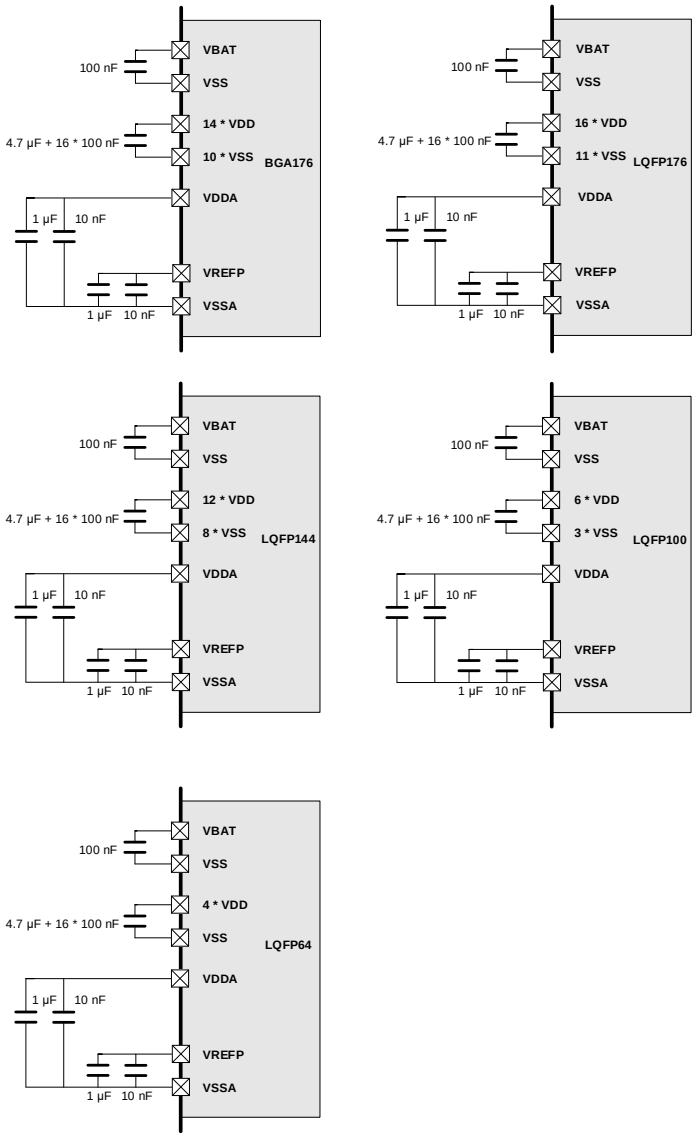
2.1.4. Power supply design

The system requires a stable power supply, and pay attention to the following precautions during development and use:

- The VDD pins must be connected to external to-ground capacitors (N * 100 nF ceramic capacitor + not less than 4.7 uF tantalum capacitor; at least a VDD pin shall be connected to a not less than 4.7 uF capacitor to GND, while other VDD pins shall be connected to 100 nF capacitors).
- The VDDA pins must be connected to external to-ground capacitors (10 nF + 1 uF ceramic capacitors are recommended).

- VREFP pin is powered externally, and a 10 nF + 1 μF ceramic capacitor should be connected to ground near the VREFP pin.

Figure 2-2. Power supply design recommended for GD32F5xx



Notes:

1. All decoupling capacitors must be installed close to V_{DD}, V_{DDA}, and V_{REFP} pins of the chip.
2. In the case of instable supply voltage or voltage drop risk of MCU, it is recommended to change 4.7 μF capacitor of V_{DD} to not less than 10 μF capacitor.

2.2. Power detection and reset

The content of this section is based on the A version of the GD32F5xx series of chips, and it is assumed that the VDD and VDDA pins are connected and powered by the same power supply.

The reset control of GD32F5xx includes three types: power reset, system reset, and backup

domain reset. Power reset is also called cold reset, which works for all systems except the backup domain. System reset works for all parts other than SW-DP controller and backup domain, including processor core and peripheral IPs. Backup domain reset works for backup area. Reset can be triggered by the external signal, internal event, and reset generator.

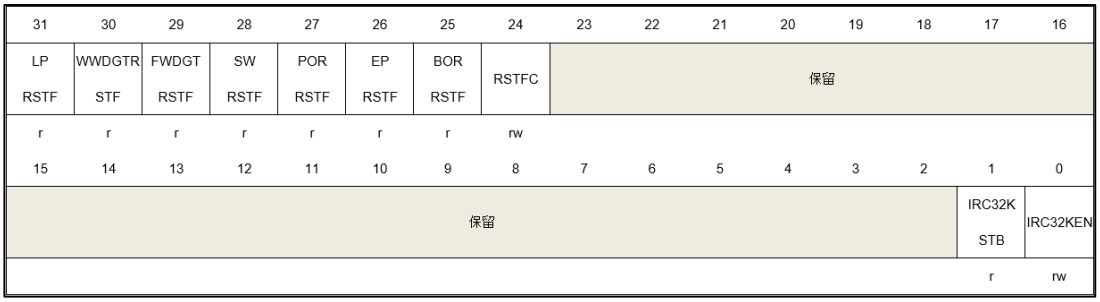
Table 2-3. Reset contents under different reset types

Reset mode	Power reset	System reset	Backup domain reset
Reset contents	All systems except the backup domain	All parts other than SW-DP controller and backup domain, including processor core and peripheral IPs	Backup area

During the power and system reset process, NRST will maintain a low level until the reset is over. In case of MCU execution failure, the waveform of NRST pin can be monitored through an oscilloscope to determine whether the chip reset event occurs continuously.

The MCU reset sources can be obtained by querying the RCU_RSTSCK register, which can only be cleared by a power-on reset. Therefore, during use, after obtaining the reset source, the reset flag can be cleared through the RSTFC control bit. Afterwards, in the event of a watchdog reset or other reset events, it can be more accurately reflected in the RCU_RSTSCK register.

Figure 2-3. RCU_RSTSCK register

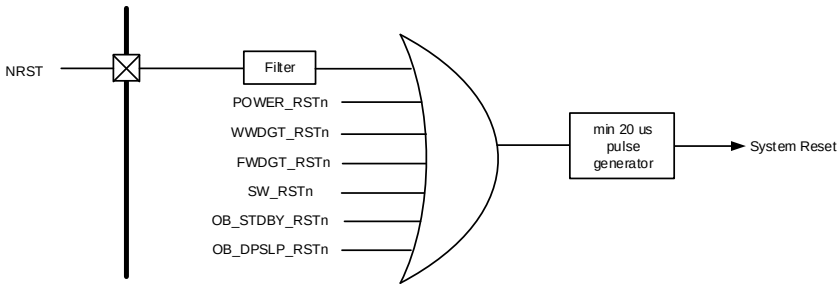


During the power supply and system reset process, NRST will maintain a low level until the reset is complete. If the MCU does not operate, an oscilloscope can be used to monitor the waveform of the NRST pin to determine if the chip is continuously experiencing reset events.

Power supply resets are divided into three categories: 1. Power-on/Power-down resets (POR / PDR resets); 2. Brown-out resets (BOR resets); 3. Resets generated by the internal reset generator after returning from standby mode.

MCU integrates a power-up / power-down reset circuit, when a reset occurs, the system reset pulse generator ensures that each reset source (external or internal) can have a low level pulse delay of at least 20 μs. The reset mothod in ***Figure 2-4. System reset circuit*** is thesystem reset.

Figure 2-4. System reset circuit



A backup domain reset is generated when one of the following events occurs:

1. The BKPRST bit in the backup domain control register is set to '1';

2. Backup domain power-on reset (when both VDD and VBAT are powered down, and then VDD or VBAT is powered up).

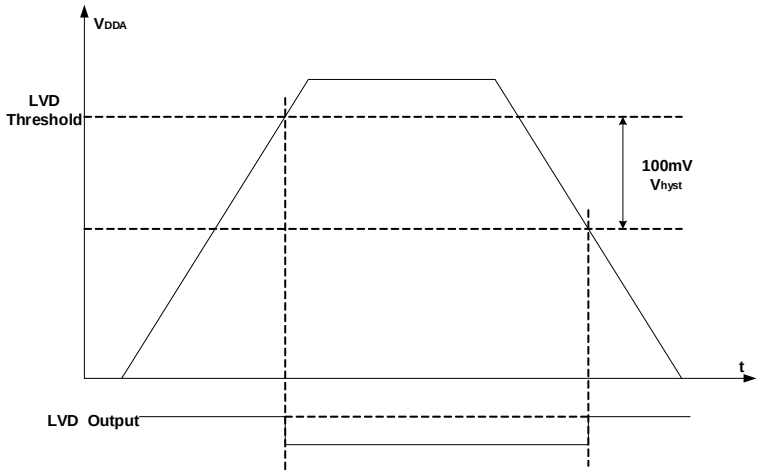
Note: When the backup domain is reset, the BKPSRAM domain will not be reset

2.2.1. LVD

LVD is used to detect whether the supply voltage of V_{DDA} is lower than the low voltage detection threshold, which is set by the LVDT[2:0] bit in the power control register (PMU_CTL). LVD is enabled by setting LVDEN. The LVDF bit in the power status register (PMU_CS) indicates whether the low voltage event connected to line 16 of EXTI occurs. An interrupt can be generated by setting line 16 of EXTI. ***Figure 2-5. LVD threshold waveform*** shows the relation between the supply voltage of V_{DDA} and the output signal of LVD. (The interrupt signal of LVD depends on the rising or falling edge configuration of line 16 of EXTI). The hysteresis voltage V_{hyst} is 100 mV.

LVD application scenario: When the power supply of MCU is subject to external interference, such as voltage drop, we can set the low voltage detection threshold (greater than the PDR value) through LVD. Once the voltage drops to the threshold, LVD interrupt is enabled, and operations such as soft reset can be set in the interrupt function to avoid other exceptions in MCU.

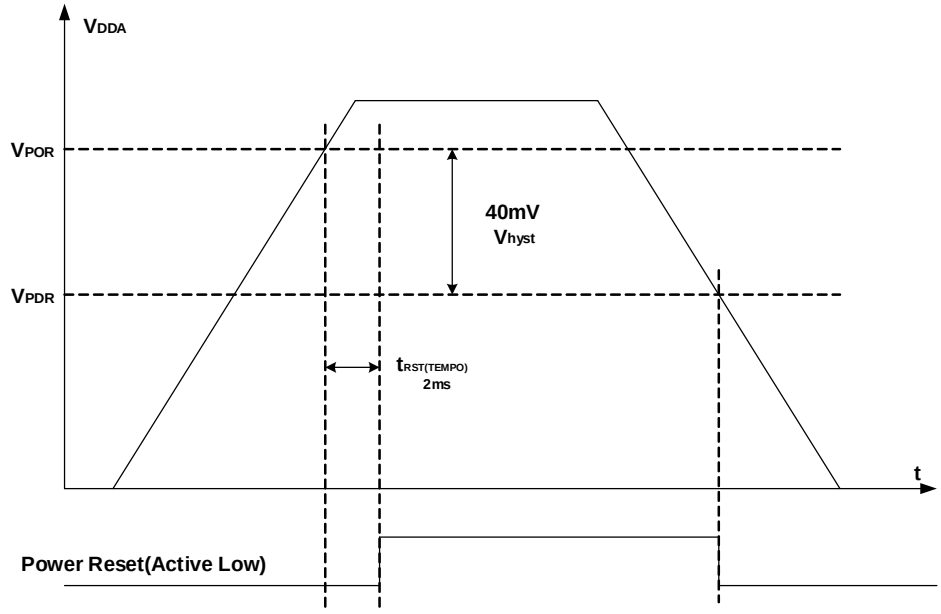
Figure 2-5. LVD threshold waveform



2.2.2. POR / PDR

The POR / PDR (power-on/power-down reset) integrated circuit in the chip detects V_{DD} and generates power reset signal to reset the entire chip except the backup domain when the voltage is lower than a specific threshold. V_{POR} is the threshold voltage of POR, typically about 1.68 V, while V_{PDR} is the threshold voltage of PDR, typically about 1.64 V. The hysteresis voltage V_{hyst} is about 40 mV. Its timing is shown in ***Figure 2-6. POR / PDR waveform***.

Figure 2-6. POR / PDR waveform

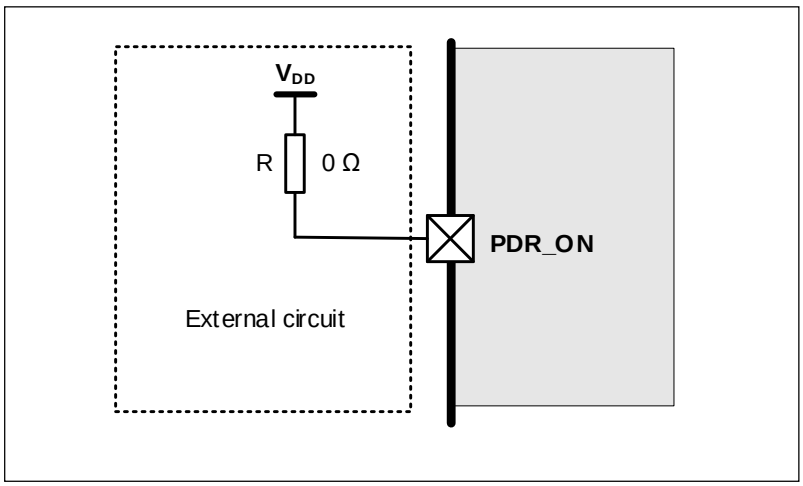


The above figure shows the relationship between power reset and V_{DDA} when BOR (Brown-out Reset) is disabled. When BOR is enabled, the impact of BOR on the power reset level must be considered. Details about BOR will be introduced in the following subsection.

QFP176, BGA176, and LQFP144 packages in GD32F5xx products are provided with PDR_ON pin to enable the POR / PDR circuit in the chip.

For effective POR and PDR in the power-on and power-down phases of the chip, the pin shall be pulled up to V_{DD} through a 0 Ω resistor, as shown in ***Figure 2-7. Recommended circuit design for PDR_ON pin***.

Figure 2-7. Recommended circuit design for PDR_ON pin

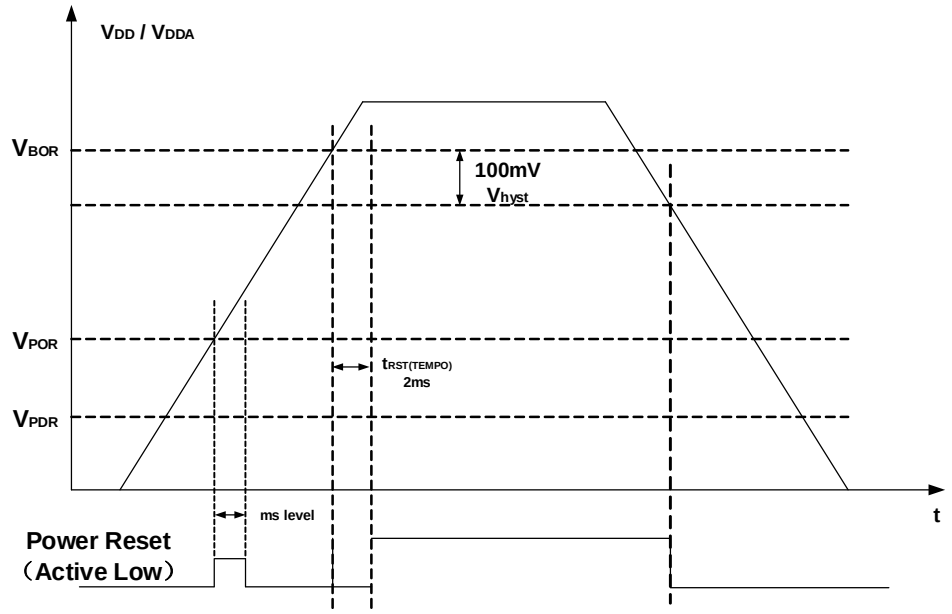


Note: The PDR_ON pin must be kept at high level. The user can flexibly adjust the value of the pull-up resistor R according to the specific scenario for a better performance.

2.2.3. BOR

The MCU of GD32F5xx also integrates the BOR circuit, this feature is turned off by default. The BOR function can be disabled, enabled, and the BOR threshold voltage can be set through the option byte BOR_TH. The BOR circuit detects V_{DD} and generates power reset signal to reset the entire chip except the backup domain when the voltage is lower than the threshold defined in the option byte BOR_TH which is not 0b11 (when BOR_TH is 0b11, the BOR function is disabled.). Whether BOR_TH is 0b11 or not, the POR/PDR circuit will always be in the detection state. ***Figure 2-8. BOR waveform*** shows the relation between the supply voltage and BOR signal. V_{BOR} represents the voltage threshold of BOR, which is defined in BOR_TH. The hysteresis voltage V_{hyst} of V_{BOR} is 100 mV.

Figure 2-8. BOR waveform



The BOR threshold can be set at three levels through BOR_TH. See ***Table 2-4. Setting VBOR threshold*** for the relation:

Table 2-4. Setting V_{BOR} threshold

Symbol	Conditions	Typ
BOR_TH=00(BOR level3)	Falling edge	2.8 V
	Rising edge	2.9 V
BOR_TH=01(BOR level2)	Falling edge	2.5 V
	Rising edge	2.6 V
BOR_TH=10(BOR level1)	Falling edge	2.2 V
	Rising edge	2.3 V
BOR_TH=11(BOR off)	-	-

Regardless of whether BOR is enabled or not, the POR / PDR (Power-on / Power-down Reset) circuit is always in a detection state. Therefore, the power reset level will be pulled high once when V_{DD} / V_{DDA} rises to VPOR. If BOR is enabled, it will quickly pull down the pulled-up power reset level until V_{DD} / V_{DDA} rises to the V_{BOR} set by the option byte BOR_TH, and then the power reset level will be pulled high again.

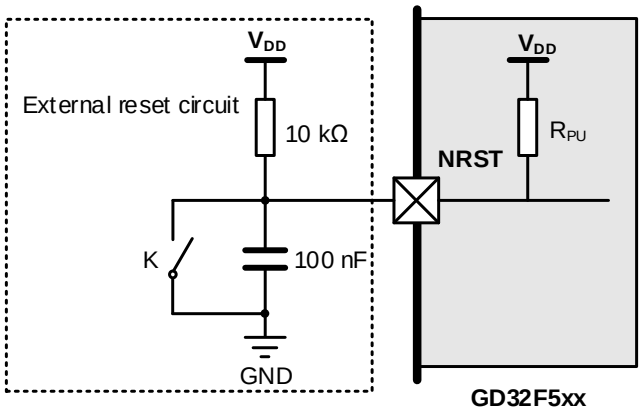
That is, when BOR is enabled and V_{DD} / V_{DDA} is on the rising edge, the voltage of the NRST pin will have a pulse when V_{DD} / V_{DDA} reaches V_{POR}. The duration of this pulse is in the order of milliseconds (the duration varies among different MCUs). This pulse does not affect the normal operation of the chip, the millisecond-level pulse as shown in ***Figure 2-8. BOR waveform***.

2.2.4. NRST pin

To prevent accidental triggering of the reset for the MCU's NRST pin, it is recommended to

place a capacitor on the NRST pin (a typical value is 100 nF).

Figure 2-9. Recommended external reset circuit

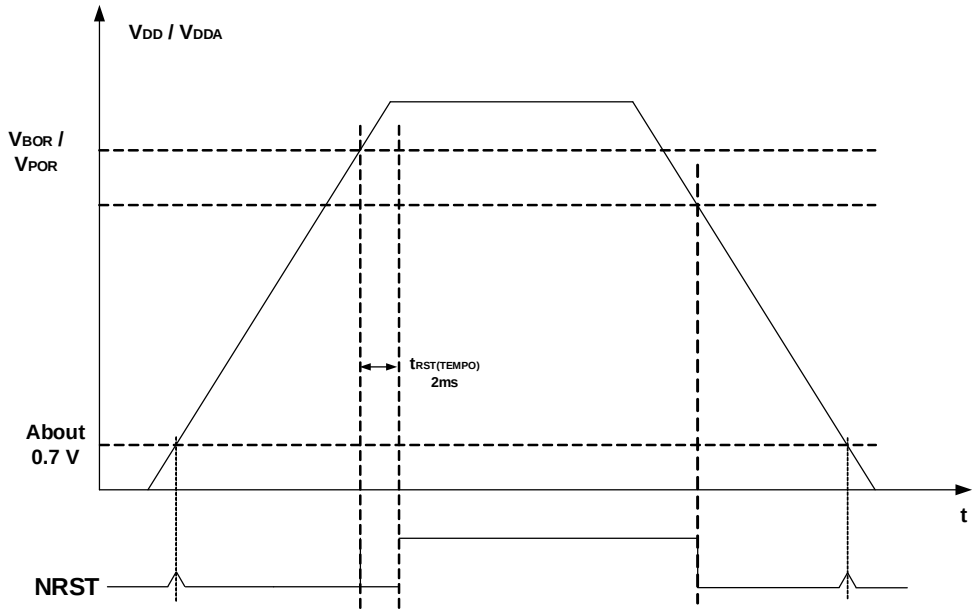


Notes:

1. 10 kΩ pull-up resistor is recommended so that voltage interference would not cause abnormal operation of the chip.
2. Considering the impact of static electricity, an ESD protection diode can be installed at the NRST pins.
3. Although there is a hardware POR circuit inside MCU, it is recommended to add an external NRST reset resistance-capacitance circuit.
4. If MCU starts abnormally (due to voltage fluctuation), the capacitance of NRST to ground can be appropriately increased to extend the MCU reset completion time and avoid the abnormal power-on sequence zone.
5. When the backup domain is reset, the BKPSRAM domain will not be reset.

Due to the threshold voltage characteristics of MOS transistors, during the power-up and power-down processes of the chip, when V_{DD} / V_{DDA} < 0.7 V, the internal pull-down MOS transistor will not pull the NRST pin low. That is, during the power-up and power-down processes of the chip, a small pulse will occur when V_{DD} / V_{DDA} is approximately 0.7 V. This pulse does not affect the normal operation of the chip, as indicated by the small pulse in ***Figure 2-10. NRST pin power / off MOS transistor pulse diagram***.

Figure 2-10. NRST pin power / off MOS transistor pulse diagram



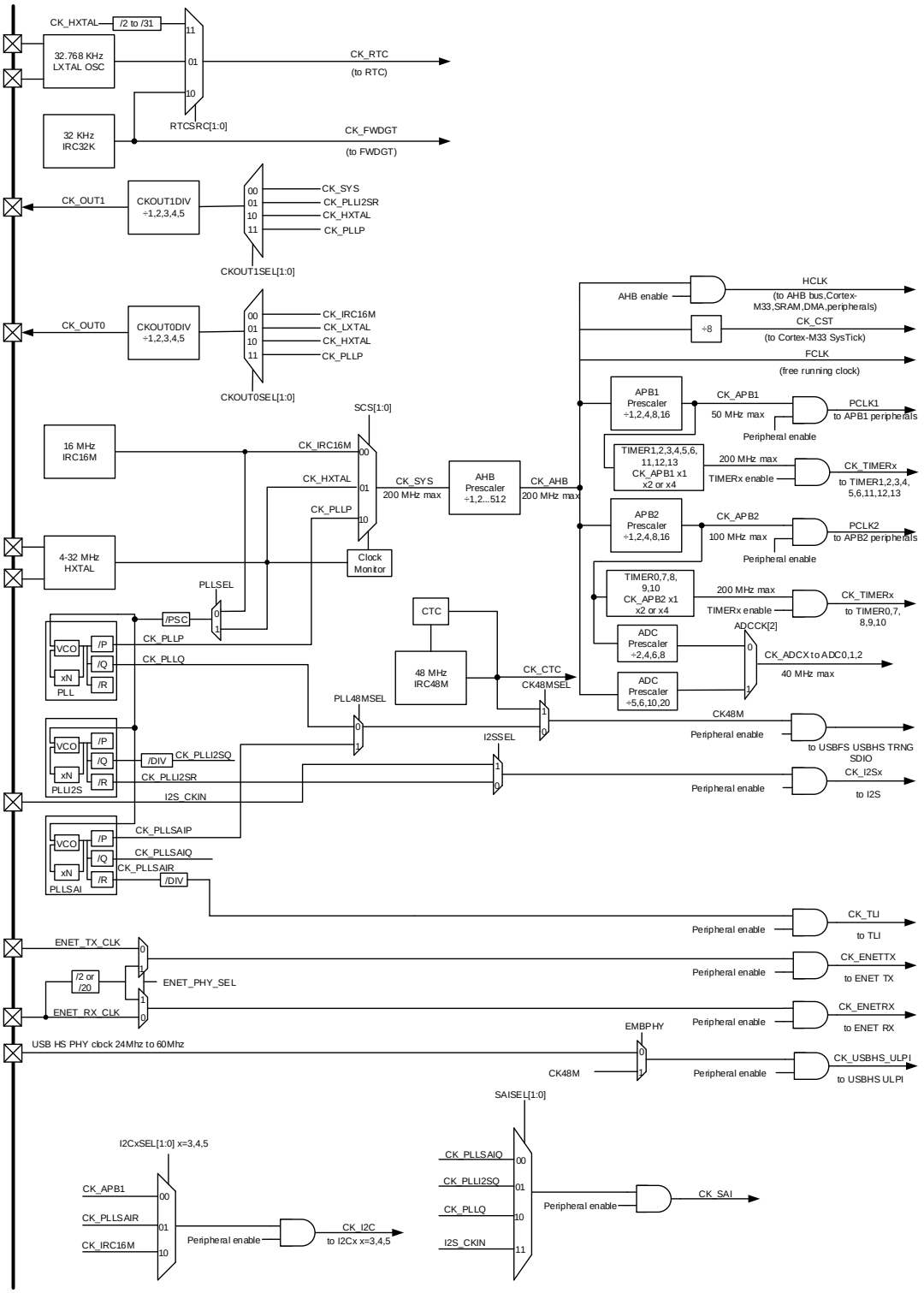
Due to the differences in power on and power off speeds, the pulse duration on the falling edge is longer than that on the rising edge, both of which are in the order of milliseconds level. If the GD32F5xx chip version differs from this document, it is recommended to contact our company to check the errata sheet.

2.3. Clock

GD32F5xx contains a complete built-in clock system, and the appropriate clock sources can be selected according to different application scenarios. The main features of the clock are as follows:

- 4 - 32 MHz high speed crystal oscillator (HXTAL)
- Internal 16 MHz RC oscillator (IRC16M)
- Internal 48 MHz RC oscillator (IRC48M)
- 32.768 kHz low speed crystal oscillator (LXTAL)
- Internal 32 kHz RC oscillator (IRC32K)
- HXTAL or IRC16M selected as the clock source of PLL
- HXTAL clock monitor

Figure 2-11. Clock tree



Note: The basic frequency of GD32F5xx MCU is up to 200 MHz.

2.3.1. External high-speed crystal oscillator clock (HXTAL)

4 - 32 MHz high-speed crystal oscillator (passive crystal) can provide an accurate master clock for the system. The crystal of specific frequency must be installed close to the HXTAL

pins, and the external resistors and matching capacitors connected to the crystal must be adjusted according to the selected oscillator parameters. HXTAL can also use the bypass input mode to input the clock source (1 - 50 MHz active crystal oscillator). In the bypass input mode, the signal is connected to the OSC_IN pin, the OSC_OUT pin remains suspended, and the Bypass function of HXTAL needs to be enabled on the software (set HXTALBPS and HXTALEN bits of the RCU_CTL control register to 1).

Figure 2-12. HXTAL external crystal circuit

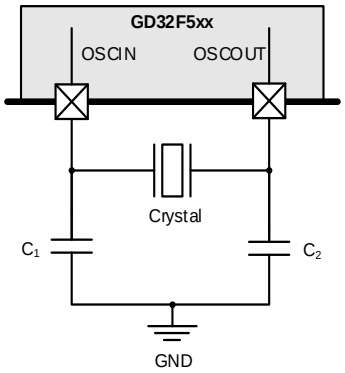
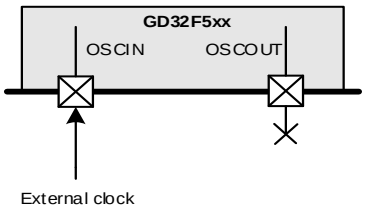


Figure 2-13. HXTAL external clock circuit in bypass mode



Notes:

1. When the bypass input mode is used, the signal is input from the OSC_IN pin, and the OSC_OUT pin remains suspended.
2. For the size of the external matching capacitor, refer to the formula: $C_1 = C_2 = 2 * (C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, typically 10 pF. When an external high-speed crystal is recommended, try to choose a crystal with a load capacitance of about 20 pF, so that the external matching capacitors C_1 and C_2 can be merely 20 pF, and the crystal shall be installed as close as possible to the crystal oscillator pins on the PCB layout.
3. C_S is the parasitic capacitance on the PCB layout and IC pins. The closer the crystal is to the MCU, the smaller the C_S, and vice versa. Therefore, in practical applications, when the crystal is far away from the MCU and works abnormally, the capacitance of the external matching capacitor can be appropriately reduced;
4. When an external high-speed crystal is used, it is recommended to connect 1 MΩ resistors in parallel at both ends of the crystal to make the crystal easier to start oscillation.
5. Accuracy: external active crystal oscillator > external passive crystal > internal IRC16M;
6. Normally, Bypass is enabled when an active crystal oscillator is used. At this time, the

high level should not be lower than 0.7 V_{DD}, and the low level should not be higher than 0.3 V_{DD}. If Bypass is not enabled, the amplitude requirements for the active crystal oscillator will be greatly reduced.

7. The wires between the resonator and MCU clock pins, namely the wires to OSC_OUT and OSC_IN pins of MCU, may have different lengths due to spatial limit of PCB layout. As a result, the stray capacitance introduced by the two PCB wires will be inconsistent, resulting in unequal load capacitance values on both sides of the resonator. This difference is required to match the actual PCB. In this case, it is recommended to contact the resonator manufacturer to measure the actual value.

2.3.2. External low-speed crystal oscillator clock (LXTAL)

LXTAL crystal is a 32.768 kHz external low-speed crystal (passive crystal), which can provide a low-power consumption and high-precision clock source for RTC. The RTC module of MCU is just like a counter whose accuracy will be affected by the crystal performance, matching capacitor, and PCB material. For better accuracy, during circuit design, it is recommended to connect PC13 to the timer input acquisition pin and set the frequency division register of RTC according to the condition of timer-based LXTAL calibration. LXTAL can also support bypass clock input (active crystal oscillator), which can be enabled by setting LXTALBPS and LXTALEN bits in RCU_BDCTL.

Figure 2-14. LXTAL external crystal circuit

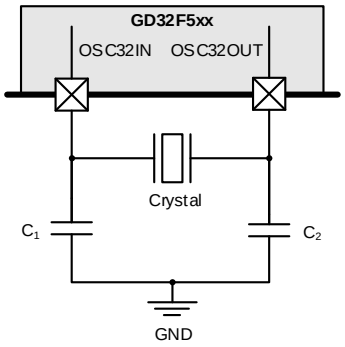
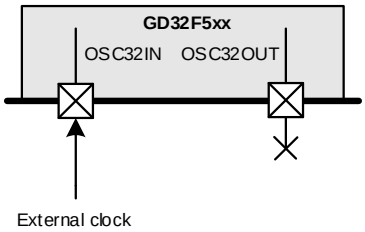


Figure 2-15. LXTAL external clock circuit in bypass mode



Notes:

1. When the bypass input mode is used, the signal is input from the OSC32_IN pin, and the OSC32_OUT pin remains suspended.

2. For the size of the external matching capacitor, refer to the formula: $C_1 = C_2 = 2 * (C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, which empirically ranges from 2 pF to 7 pF and is recommended to be 5 pF for calculation. When an external crystal is recommended, try to choose a crystal with a load capacitance of about 10 pF, so that the external matching capacitors C_1 and C_2 can be merely10 pF, and the crystal shall be installed as close as possible to the crystal oscillator pins on the PCB layout.
3. When IRC32K is selected as the clock source of RTC that is separately powered by external V_{BAT}, RTC will stop counting if MCU is powered down. After MCU is powered on again, RTC will keep counting starting from the previous count value. If external V_{BAT} shall separately power RTC and RTC can still perform normal counting after MCU is powered down, LXTAL must be selected as the clock source of RTC.
4. The drive capability of LXTAL can be set in MCU. If it is difficult for an external low-speed crystal to start oscillation during actual debugging, the drive capability of LXTAL can be adjusted to high drive capability.
5. The wires between the resonator and MCU clock pins, namely the wires to OSC_OUT and OSC_IN pins of MCU, may have different lengths due to spatial limit of PCB layout. As a result, the stray capacitance introduced by the two PCB cables will be inconsistent, resulting in unequal load capacitance values on both sides of the resonator. A difference is required to match the actual PCB. In this case, it is recommended to contact the resonator manufacturer to measure the actual value.

2.3.3. Clock output capability (CKOUT)

GD32F5xx MCU can output 32 kHz to 200 MHz clock signal. Different clock signals can be selected by setting the CK_OUT0 clock source selection bit field CKOUT0SEL in the clock configuration register 0(RCU_CFG0). CK_OUT1 clock output source can be selected by setting the CKOUT1SEL bit filed in the clock configuration register RCU_CFG0. GPIO pins shall be set in the alternate function I/O (AFIO) mode to output the selected clock signal. The IO ports of CK_OUT0 and CK_OUT1 are PA8 and PC9, respectively.

Table 2-5. Clock source selection for clock output 0

Clock source selection bit field for clock output 0	Clock source
00	CK_IRC16M
01	CK_LXTAL
10	CK_HXTAL
11	CK_PLLP

Table 2-6. Clock source selection for clock output 1

Clock source selection bit field for clock output 1	Clock source
00	CK_SYS
01	CK_PLLI2SR

Clock source selection bit field for clock output 1	Clock source
10	CK_HXTAL
11	CK_PLLP

2.3.4. HXTAL clock monitor (CKM)

The HXTAL clock monitoring function can be enabled by setting the HXTAL clock monitoring enable bit CKMEN in the control register RCU_CTL. The function must be enabled after the HXTAL boot delay is over and disabled after HXTAL stops. Once an HXTAL fault is monitored, HXTAL will be automatically disabled, and the HXTAL clock blocking interrupt flag bit CKMIF in the interrupt register RCU_INT will be set to 1, which will generate the HXTAL fault event. The fault-induced interrupt is connected to the non-maskable interrupt (NMI) of Cortex®-M33. In the case of the failure of HXTAL that is selected as the clock source of the system or PLL, IRC16M will be selected as the clock source of the system and PLL will be automatically disabled.

2.3.5. PLL spread spectrum (SSCG)

PLL of GD32F5xx integrates the clock spread spectrum function (only for main PLL) to effectively reduce EMI and PLL energy at the master clock frequency point and its odd harmonics. Calculate MODCNT and MODSTEP according to the set modulation frequency f_{mod}, peak modulation amplitude mdamp (see ***Table 2-7. PLL spread spectrum clock generation (SSCG) characteristics*** for their ranges), as well as formulae (2-1) and (2-2), and fill the PLL clock spread spectrum control register (RCU_PLLSSCTL) with them. Note that the product of MODCNT and MODSTEP can not be more than 2^15-1; however if it is, the peak modulation amplitude mdamp shall be reduced for re-calculation.

Table 2-7. PLL spread spectrum clock generation (SSCG) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{mod}	Modulation frequency	—	—	—	10	kHz
mdamp	Peak modulation amplitude	—	—	—	2	%
MODCNT* MODSTEP	—	—	—	—	2^{15}-1	—

MODCNT and MODSTEP are calculated by using the following formulae:

$$MODCNT = round(f_{PLLIN}/4/f_{mod}) \quad (2\text{-}1)$$

$$MODSTEP = round(mdamp*PLLN*2^{14}/(MODCNT*100)) \quad (2\text{-}2)$$

Where, f_{PLLIN} is the input clock frequency of PLL, f_{mod} is the modulation frequency of spread spectrum, mdamp is the modulation amplitude of spread spectrum in percentage, PLLN is the clock frequency multiplication factor of PLL.

For example, if the reference clock source HXTAL of PLL is 8 MHz and pre-divided frequency PLLM is 4, f_{PLLIN} is 2 MHz. By setting PLLN to 200 (400 MHz VCO frequency is divided by two to obtain the system clock frequency of 200 MHz), the modulation frequency of spread

spectrum to 10 KHz, and the modulation amplitude to 2%, MODCNT and MODSTEP are calculated to be 50 and 1311 respectively. The requirement is not met as the product of MODCNT and MODSTEP is greater than 2^{15}-1. However if the modulation amplitude is reduced to 1%, MODCNT and MODSTEP are calculated to be 50 and 655 respectively. The requirement is met as the product of MODCNT and MODSTEP is 32750, lower than 2^{15}-1.

According to SS_TYPE setting in the RCU_PLLSSCTL register, two modulation types of spread spectrum can be selected, namely central spread spectrum and downward spread spectrum, and the output frequency of PLL will change according to the following waveform.

Figure 2-16. Central spread spectrum

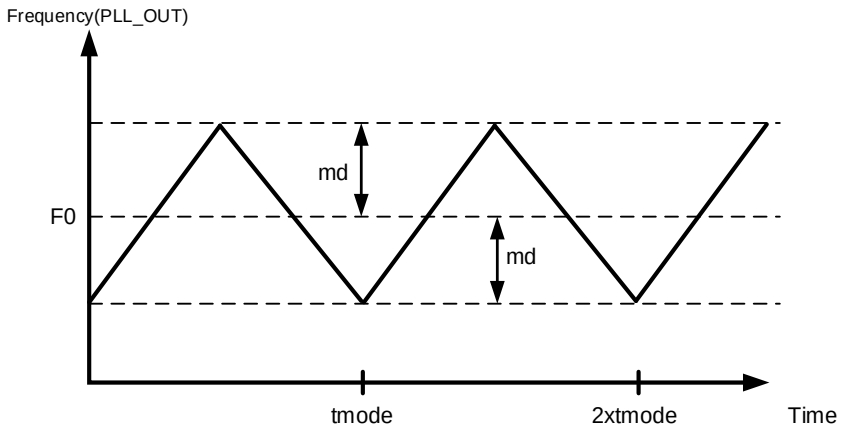
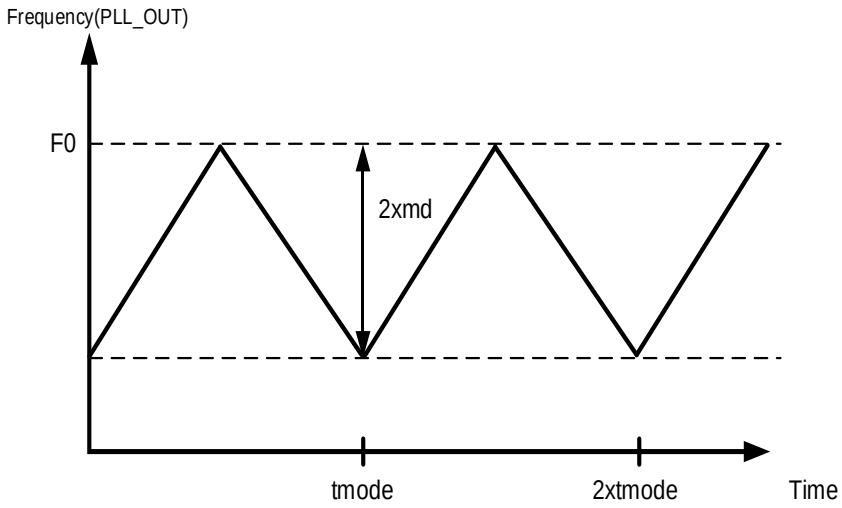


Figure 2-17. Downward spread spectrum



Note: If the spread spectrum function of PLL is enabled, the system clock frequency will fluctuate, which may lead to abnormal operation of peripherals with high requirements on clock accuracy. For example, when the clock signal is output via MCU IO, as the clock source of USB or Ethernet, PHY may perform abnormal operation. USB can use an internal 48 MHz clock (CTC calibration is recommended) or an external clock by being connected to high-speed PHY, while Ethernet must use an external clock.

2.4. Boot configuration

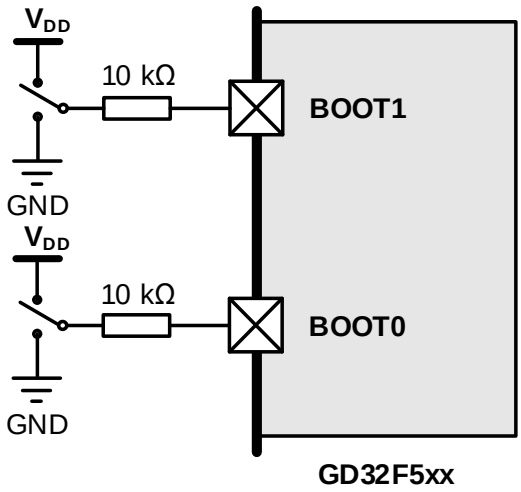
GD32F5xx provides three boot modes, which can be selected and determined through the BOOT0 bit and BOOT1 pin. To run the user program during circuit design, the BOOT0 pin cannot be suspended, so it is recommended to connect it to GND through a 10 kΩ resistor. To run System Memory to update the program, it is required to connect the BOOT0 pin to a high voltage and the BOOT1 pin to a low voltage. After the update is completed, it is necessary to connect the BOOT0 pin to a low voltage and power it on before the user program can be run. The SRAM execution program is mostly run in the debugging state.

The embedded Bootloader is stored in the system memory space and is used to reprogram the FLASH memory. Bootloader can interact with the outside world through USART0 (PA9 and PA10), USART2 (PB10 and PB11, PC10 and PC11, and PE8 and PD15), or USBFS (PA11 and PA12) in the slave mode.

Table 2-8. BOOT mode

BOOT mode	BOOT1	BOOT0
Main Flash Memory	x	0
System Memory	0	1
On Chip SRAM	1	1

Figure 2-18. Recommended BOOT circuit design



Notes:

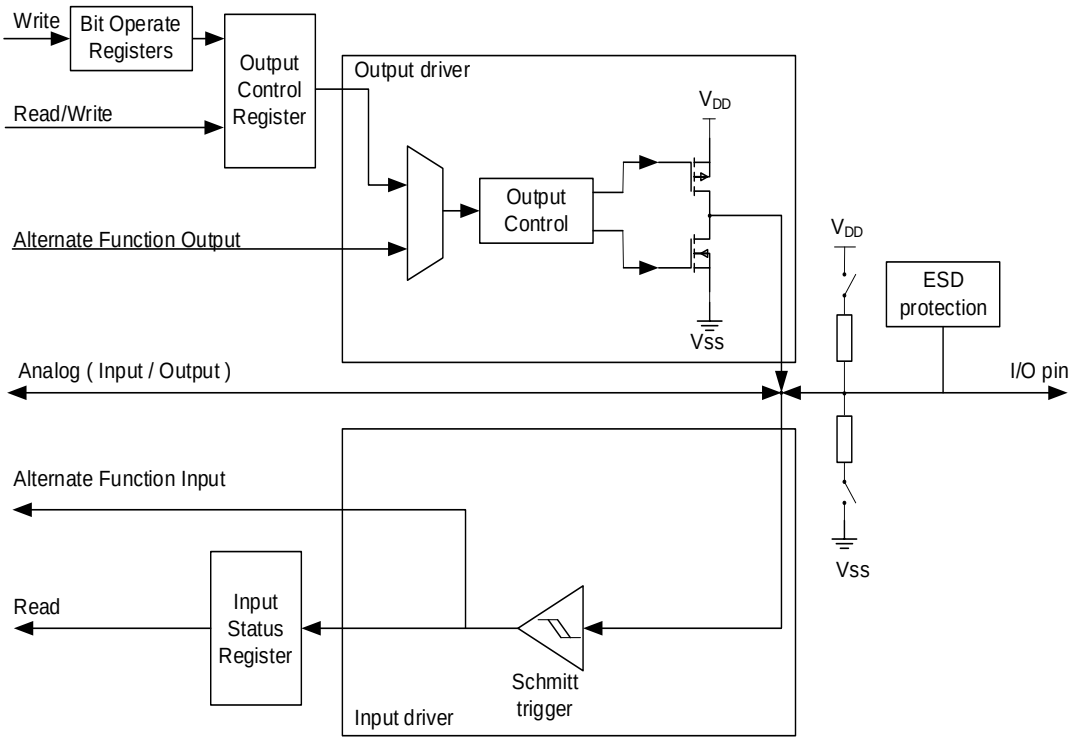
1. After MCU runs, if the BOOT state is changed, it will take effect only after the system is reset.
2. Once the BOOT1 pin states are sampled, they can be released for other purposes.

2.5. Typical peripheral modules

2.5.1. GPIO circuit

GD32F5xx can support up to 140 general purpose I/O (GPIO) pins, including PA0 to PA15, PB0 to PB15, PC0 to PC15, PD0 to PD15, PE0 to PE15, PF0 to PF15, PG0 to PG15, PH0 to PH15, and PI0 to PI11. Each pin can be set separately through the register. The basic structure of the GPIO pin is shown in ***Figure 2-19. Basic structure of standard IO***:

Figure 2-19. Basic structure of standard IO



Notes:

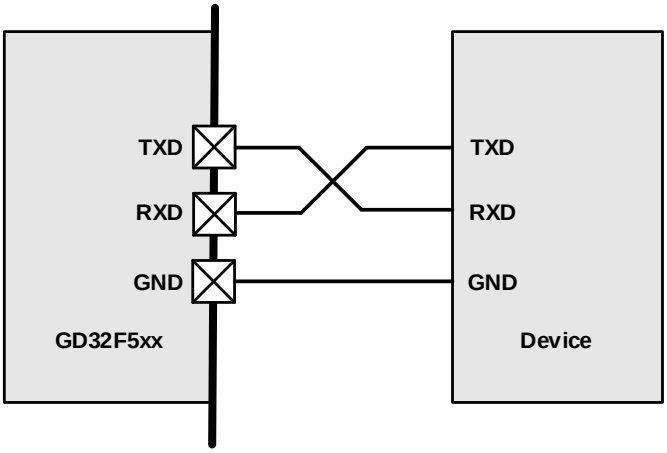
1. IO pins are divided into pins resistant to 5 V and pins non-resistant to 5 V, so pay attention to distinguishing voltage resistance of IO pins when using them. For GD32F5xx chips, PA4 and PA5 pins are non-resistant to 5 V, other pins are resistant to 5 V.
2. When IO pins resistant to 5 V are directly connected to 5 V, it is recommended to set them in open-drain mode and output high level through external pull-up.
3. Each GPIO pin can be set in the software in output (push-pull or open-drain) mode, input mode, backup mode for peripherals, or analog mode.
4. As the alternate function has not been activated during or after reset, all GPIO pins are set in floating input mode, where the pull-up (PU)/pull-down (PD) resistors are disabled. To achieve consistent power consumptions, it is recommended that all IO pins be set in analog input mode and then modified to the corresponding mode according to application requirements (also for pins in the chip that are not led out).

5. To improve the EMC performance, unused IO port pins are recommended to be pulled up or down by the hardware;
6. As four IO pins (namely PC13, PC14, PC15, and PI8) have poor drive capability and limited current output capability, they can not work beyond 2 MHz after being set in output mode.
7. Peripheral interrupt/event line can be used only if the pins are set in input mode.
8. It is recommended to install ESD protection circuit close to the external end for pins that need to be connected to external devices, switches, or keys.

2.5.2. USART/UART circuit

GD32F5xx products provide four USARTs (USART0, USART1, USART2, and USART5) and four UARTs (UART3, UART4, UART6, and UART7). See ***Figure 2-20. USART/UART reference circuit*** for cross connection of pins when using USART/UART.

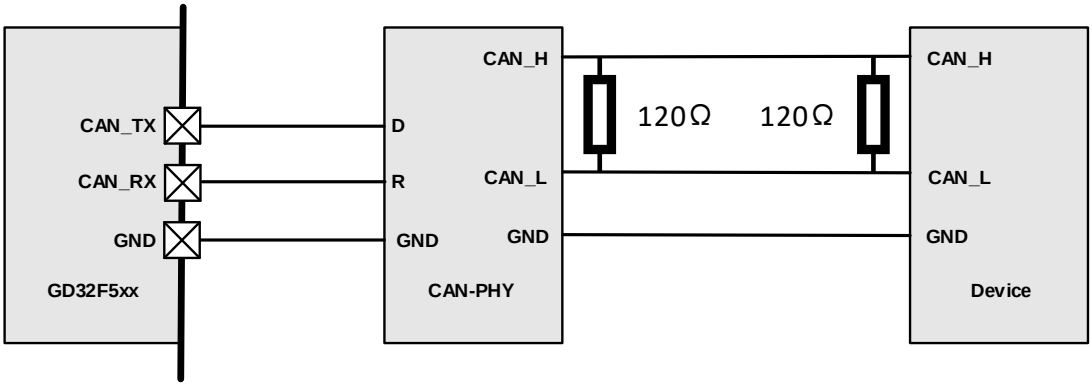
Figure 2-20. USART/UART reference circuit



2.5.3. CAN circuit

GD32F5xx chips provide two CAN communication peripherals (CAN0 and CAN1), as shown in ***Figure 2-21. CAN reference circuit***.

Figure 2-21. CAN reference circuit



For two 120 Ω impedance matching resistors shown in the above figure, their resistance

values and whether they are needed can be determined on a case-by-case basis.

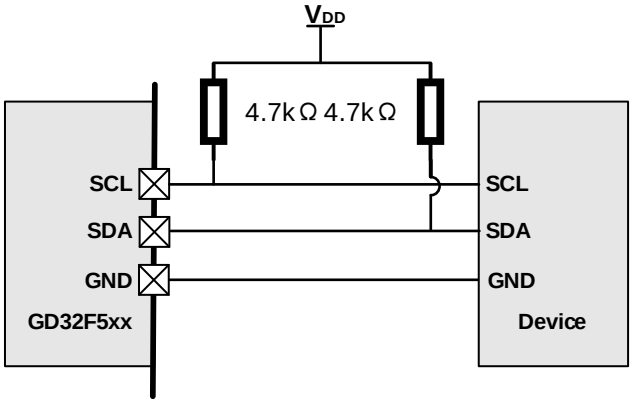
The impedance matching resistors exert three functions during CAN communication:

1. Improve the anti-interference capability.
2. Prevent signal reflection for higher signal quality.
3. Ensure that the rising/falling edge is quickly reached for the bus.

2.5.4. I2C circuit

GD32F5xx chips provide six I2C peripherals: I2C0, I2C1, and I2C2 can work in standard mode (up to 100 KHz) and fast mode (up to 400 KHz). Besides standard and fast modes, I2C3, I2C4, and I2C5 can work in fast mode plus (up to 1 MHz provided that I2CxFMP(x = 3, 4, 5) is enabled in SYSCFG_CFG1). As both SDA and SCL are bidirectional lines, all I2C channels can work in master or slave mode. They can also work in multi-master mode. The I2C interface module can also work in DMA mode, which can effectively alleviate the burden on CPU.

Figure 2-22. I2C reference circuit



For connection to the output pole of the I2C bus device, considering wired-AND, it is required to set a high level when idle.

For the OC/OD circuit, its reaction speed and power consumption depend on the pull-up resistor. The pull-up resistor with small resistance leads to fast reaction and steep signal edge (namely, good signal quality) but high power consumption. On the contrast, the pull-up resistor with large resistance leads to low power consumption but slow circuit reaction and gentle signal edge (namely poor signal quality).

Table 2-9. Reference relation between transmission mode and pull-up resistor

Transmission mode	Pull-up resistor (kΩ)
Standard mode	4.7
Fast mode	2.2
Fast mode plus	1.5

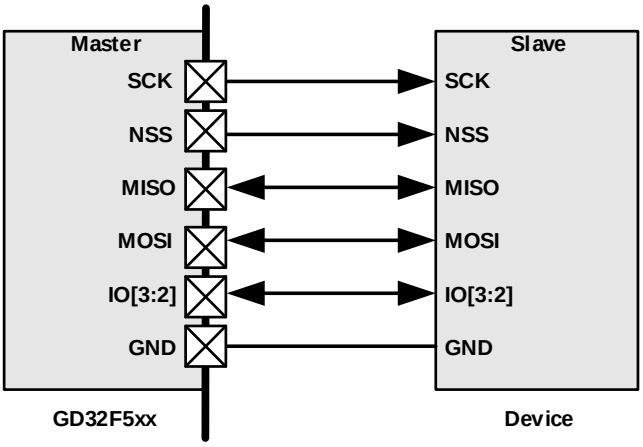
Considering actual wiring of I2C and complex conditions of the circuit board, the resistances of the pull-up resistor listed in ***Table 2-9. Reference relation between transmission mode***

and pull-up resistor are for reference only. In actual use, a string set can be installed between SDA and SCL to adjust the signal quality.

2.5.5. SPI circuit

GD32F5xx chips provide six SPIs. SPI5 can be set through registers and extended to four-wire mode. Except the SPI in four-wire mode, all SPI channels can work in master or slave mode. SPI5 in four-wire mode can only work as a host. It can work as a slave in the mode other than four-wire mode.

Figure 2-23. SPI reference circuit in four-wire mode



The above figure is only for reference when SPI5 works in four-wire mode. At that time, GD32F5xx chip can only work as hosts. The following four connection methods in typical work modes are available for general SPI after being properly set through registers. GD32F5xx chips can work as masters or slaves in the following work modes.

Figure 2-24. Connection of SPI in typical full duplex mode

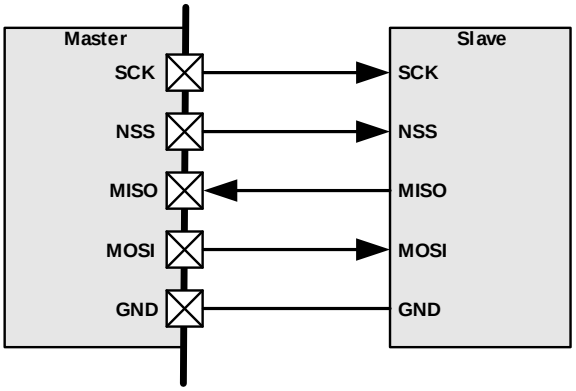


Figure 2-25. Connection of SPI in typical simplex mode (master: receiving; slave:

transmitting)

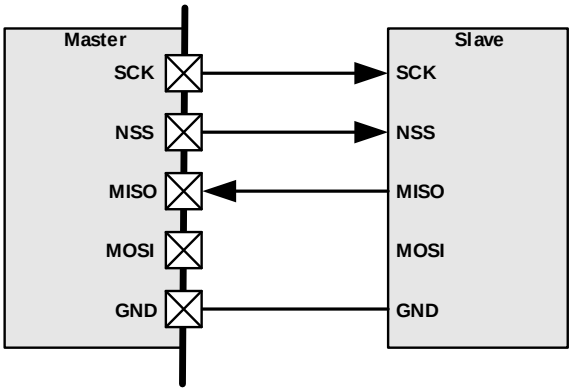


Figure 2-26. Connection of SPI in typical simplex mode (master: transmitting; slave: receiving)

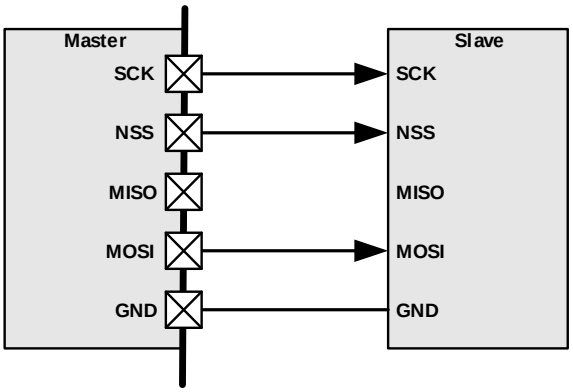
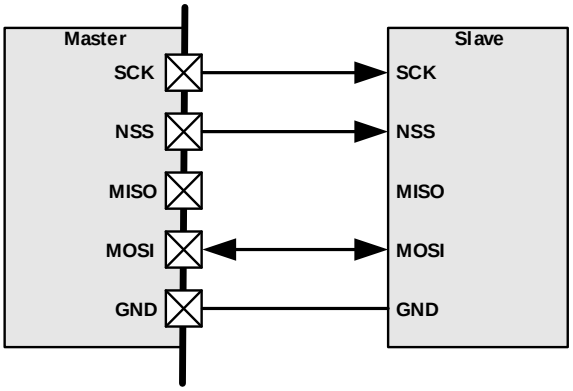


Figure 2-27. Connection of SPI in typical bidirectional line mode



2.5.6. Battery circuit

When V_{DD} is powered down, normal operation of the backup domain of GD32F5xx chips can be kept by powering the V_{BAT} pin. The following circuits are for reference when an external battery is used to power the V_{BAT} pin.

Figure 2-28. Non-rechargeable battery reference circuit (1)

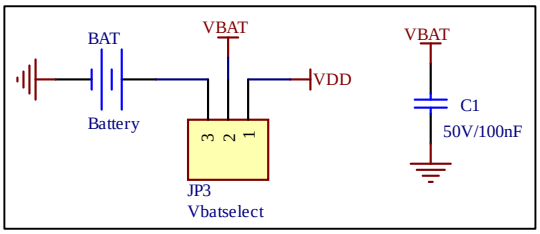


Figure 2-29. Non-rechargeable battery reference circuit (2)

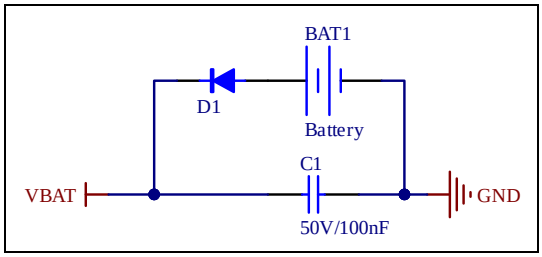
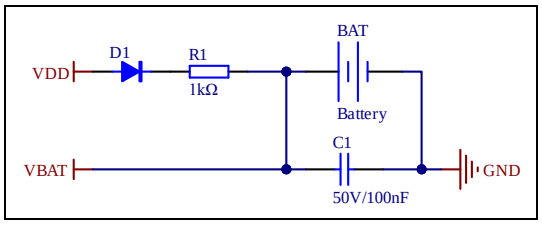


Figure 2-30. Rechargeable battery reference circuit



When referring to the above circuits, pay attention to the battery voltage, voltage drop of the diode, and supply voltage range of the V_{BAT} pin against overvoltage or undervoltage. For the resistor in the rechargeable battery reference circuit, its resistance is selected according to the battery characteristics.

2.5.7. ADC circuit

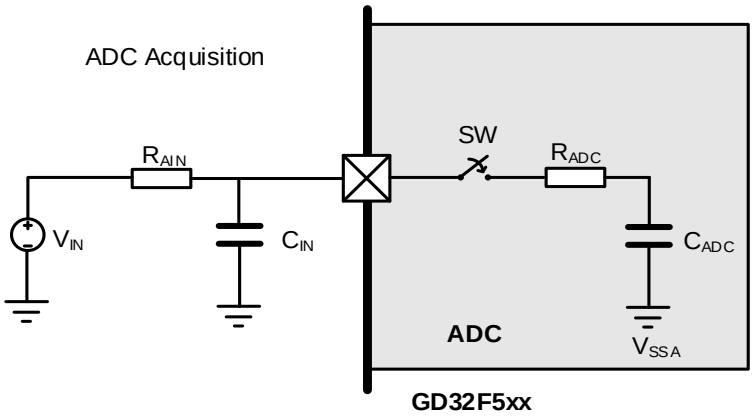
GD32F5xx integrates a 12-bit SAR ADC with up to 19 channels and can measure 16 external signal sources, two internal signal sources, and a signal source for monitoring the external battery voltage (V_{BAT}). Internal signal is measured through the temperature sensor channel (ADC0_CH16) and internal reference voltage input channel (ADC0_CH17), while external signal is measured through the supply pin input channel (ADC0_CH18) for monitoring the external battery voltage (V_{BAT}). The temperature sensor reflects temperature changes and is not suitable for measuring absolute temperature. To measure the accurate temperature, an external temperature sensor must be used. The internal reference voltage V_{REFINT} provides a stable output voltage (1.2 V) for ADC and is internally connected to ADC0_CH17. A pin is provided for monitoring the external battery voltage (V_{BAT}), which is converted to $V_{BAT}/4$.

If ADC collects the external input voltage during use and the sampled data fluctuates greatly, it may be caused by interferences due to power supply fluctuation. In this case, calibration can be done by sampling the internal VREFINT to derive the external sampled voltage.

When designing the ADC circuit, it is recommended to install a small capacitor of 500 pF at

the ADC input pins.

Figure 2-31. Design of ADC acquisition circuit



To obtain better conversion results, it is recommended to reduce f_{ADC} as much as possible during use, try to select a large value of sampling period, and minimize the input impedance when designing external circuits. If necessary, use the op-amp following to reduce the input impedance. When f_{ADC} is 40 MHz, the relation between the input impedance and the sampling period is as follows.

Table 2-10. Relation between sampling period and external input impedance when f_{ADC} is 40 MHz

T_s (cycles)	t_s (us)	$R_{AIN\ max}$ (kΩ)
3	0.075	0.55
15	0.375	4.65
28	0.7	9.15
55	1.375	18.43
84	2.1	28.46
112	2.8	38.1
144	3.6	49.17
480	12	N/A

2.5.8. DAC circuit

The digital/analog converter of GD32F5xx MCU can convert 12-bit digital data into the output voltage on external pins. The data can be in 8-bit or 12-bit mode and left-aligned or right-aligned mode. When the external trigger is enabled, DMA can be used to update the digital data at the input. When the voltage is output, the DAC output buffer can be enabled to obtain higher drive capability. Two channels of each DAC can work separately or concurrently.

Table 2-11. Description of related DAC pins

Name	Description	Signal type
V_{DDA}	Analog power	Input analog power
V_{SSA}	Analog power ground	Input analog power ground
V_{REFP}	DAC positive reference voltage, 1.71 V ≤ V_{REFP} ≤ V_{DDA}	Input analog positive reference voltage
DAC_OUTx	DACx analog output	Analog output signal

Before the DAC module is enabled, the GPIO pin shall be set in analog mode.

2.5.9. USB circuit

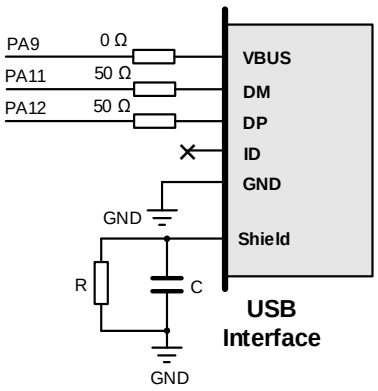
GD32F5xx MCU comes with two USB interfaces, USBFS interface and USBHS interface. The USBFS interface has a built-in full-speed USB PHY, so an external PHY chip is no longer needed. The USBHS interface provides a ULPI interface for an external USB PHY and also has a built-in full-speed USB PHY. Therefore, an external USB PHY is no longer needed for full-speed operation. If an external high-speed ULPI PHY is used, the USBHS interface can support high speed at most.

The internal clock may be unable to reach the accuracy of not less than 500 ppm, which is specified in the USB protocol, so it is recommended to use an external crystal or active crystal oscillator as the clock source of the USB module when using the USB function.

The USB of GD32F5xx can be designed as a USB device or a USB host. When it is designed as the USB device, if the VBUSIG control bit in the USBFS_GCCFG register is set as 1, PA9 shall not be connected to the V_{BUS} line; however, if it is set as 0, PA9 must be connected to the V_{BUS} line.

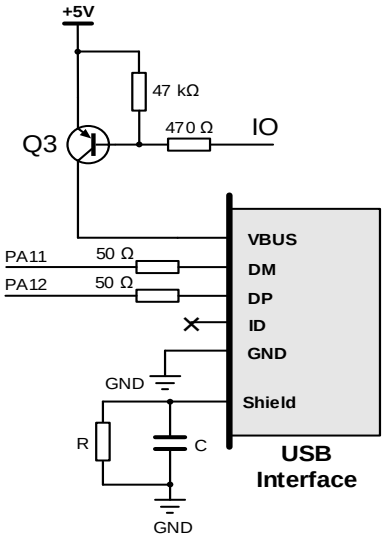
For better ESD performance of USB during circuit design, it is recommended to design a resistance-capacitance discharge isolation circuit for the USB shell.

Figure 2-32. USBFS-Device recommended reference circuit



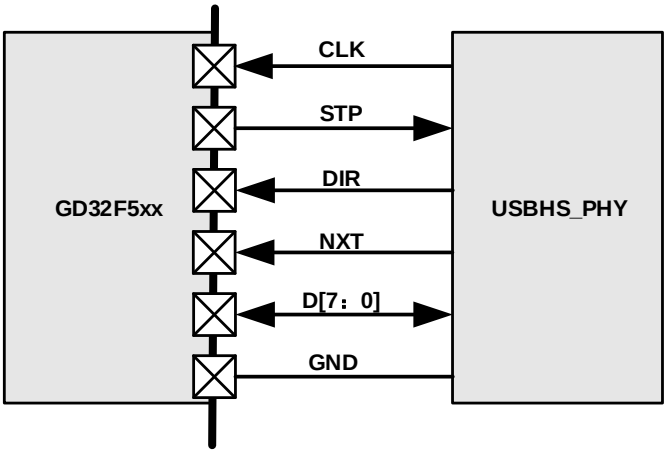
Recommendation: R = 1 MΩ, C = 4700 pF.

Figure 2-33. USBFS-Host recommended reference circuit



Recommendation: R = 1 MΩ, C = 4700 pF.

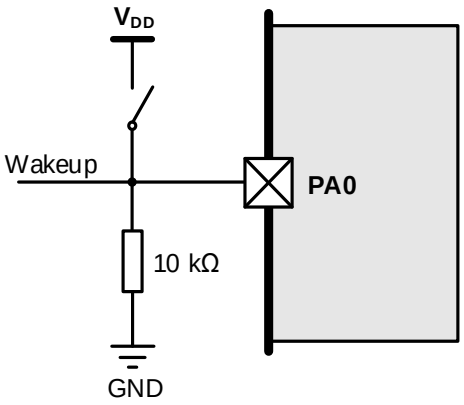
Figure 2-34. USBHS recommended reference circuit



2.5.10. Wake-up circuit in standby mode

GD32F5xx supports three low power modes, namely sleep mode, deep sleep mode, and standby mode. MCU in standby mode consumes the least power, but wake-up of MCU in such mode costs the longest time. MCU in standby mode can be woken up through the rising edge of the WKUP pin by setting the WUPEN bit in the PMU_CS register rather than the corresponding GPIO. The reference circuit design of the WKUP wake-up pin is as follows:

Figure 2-35. Recommended circuit design for external wake-up pin in standby mode

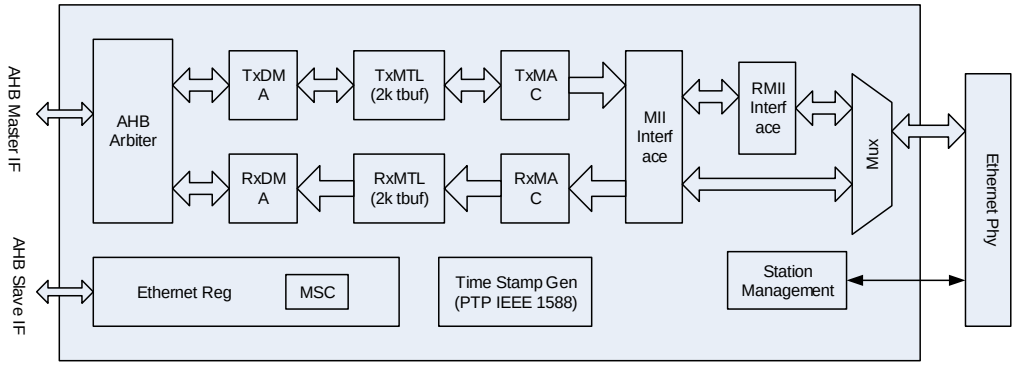


Note: During circuit design in this mode, if there are series resistors between the WKUP pin and V_{DD}, additional power consumption may be generated.

2.5.11. Ethernet circuit

GD32F5xx products support Ethernet peripherals, including 10/100 Mbps Ethernet media access controller (MAC), where DMA is used for optimized transmitting and receiving of data frames and the standard interface for communication between the media independent interface (MII)/reduced media independent interface (RMII) and PHY is supported for transmitting and receiving of Ethernet data frames. The Ethernet module follows IEEE 802.3-2002 and IEEE 1588-2008.

Figure 2-36. Ethernet module



When using the Ethernet module, make sure that the set clock frequency is not less than 25 MHz.

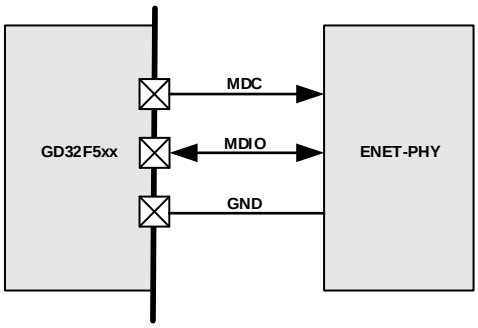
Among Ethernet peripherals, the site management interface (SMI) is used to access and set PHY and communicate with external PHY through MDC clock line and MDIO data line to access any register of any PHY. SMI can support up to 32 PHYs but can only access a register of a PHY at a time. The MDC clock line and MDIO data line function as follows:

- MDC: It refers to the clock signal with a maximum frequency of 2.5 MHz. When idle, the signal is in the low level state. With a minimum period of 400 ns, the signal is in high or

low level state for a minimum time of 160 ns during data transmission.

- MDIO: It is used for data transmission with PHY and data receiving/transmitting together with MDC clock line.

Figure 2-37. SMI circuit



The default and remapping functions and the setting of the pins for the MAC module in MII/RMII mode are listed in ***Table 2-12. Ethernet signal in MII mode*** and ***Table 2-13. Ethernet signal in RMII mode***.

Table 2-12. Ethernet signal in MII mode

Signal	Pin 1	Pin 2	Pin mode (AF11)
MDC	PC1	-	Push-pull multiplexed output
MII_TXD2	PC2	-	Push-pull multiplexed output
MII_TX_CLK	PC3	-	Floating input in reset state
MII_CRS	PA0	PH2	Floating input in reset state
MII_RX_CLK	PA1	-	Floating input in reset state
MDIO	PA2	-	Push-pull multiplexed output
MII_COL	PA3	PH3	Floating input in reset state
MII_RX_DV	PA7	-	Floating input in reset state
MII_RXD0	PC4	-	Floating input in reset state
MII_RXD1	PC5	-	Floating input in reset state
MII_RXD2	PB0	PH6	Floating input in reset state
MII_RXD3	PB1	PH7	Floating input in reset state
PPS_OUT	PB5	PG8	Push-pull multiplexed output
MII_TXD3	PB8	PE2	Push-pull multiplexed output
MII_RX_ER	PB10	PI10	Floating input in reset state
MII_TX_EN	PB11	PG11	Push-pull multiplexed output
MII_TXD0	PB12	PG13	Push-pull multiplexed output
MII_TXD1	PB13	PG14	Push-pull multiplexed output

Table 2-13. Ethernet signal in RMII mode

Signal	Pin 1	Pin 2	Pin mode (AF11)
MDC	PC1	-	Push-pull multiplexed output
REF_CLK	PA1	-	Floating input in reset state
MDIO	PA2	-	Push-pull multiplexed output
CRS_DV	PA7	-	Floating input in reset state

Signal	Pin 1	Pin 2	Pin mode (AF11)
RMII_RXD0	PC4	-	Floating input in reset state
RMII_RXD1	PC5	-	Floating input in reset state
PPS_OUT	PB5	PG8	Push-pull multiplexed output
RMII_TX_EN	PB11	PG11	Push-pull multiplexed output
RMII_TXD0	PB12	PG13	Push-pull multiplexed output
RMII_TXD1	PB13	PG14	Push-pull multiplexed output

Note: Make sure that only one pin (pin 1 or pin 2) is mapped to AF11 for any interface (MII/RMII) in the application.

The following two recommended circuits for the Ethernet peripherals supported by GD32F5xx products are for reference.

Figure 2-38. Recommended circuit for MII

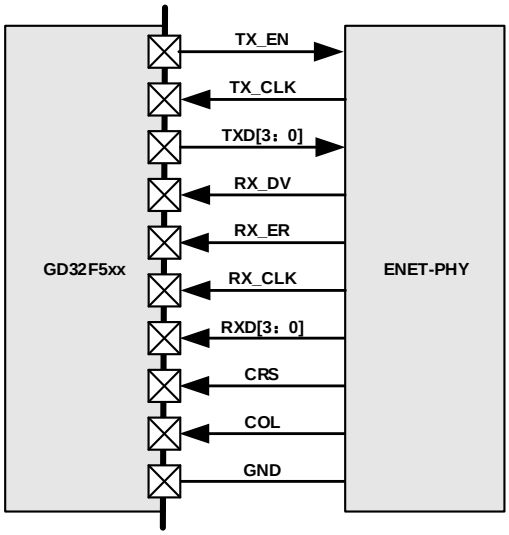
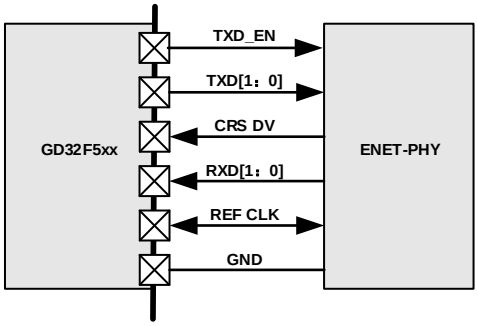


Figure 2-39. Signal line for RMII



2.6. Download debug circuit

The core of GD32F5xx supports JTAG debug interface and SWD interface. The standard JTAG interface is a 20-pin interface, including 5-wire signal interface. The standard SWD interface is a 5-pin interface, including 2-wire signal interface.

Note: After resetting, the debug related ports are in input PU/PD mode, where:

PA15: JTDI is in pull-up mode.

PA14: JTCK/SWCLK is in pull-down mode.

PA13: JTMS/SWDIO is in pull-up mode.

PB4: NJTRST is in pull-up mode.

PB3: JTDO is in floating mode.

Table 2-14. Allocation of JTAG download debug interfaces

Alternate function	GPIO port
JTMS	PA13
JTCK	PA14
JTDI	PA15
JTDO	PB3
NJTRST	PB4

Figure 2-40. Recommended JTAG wiring reference design

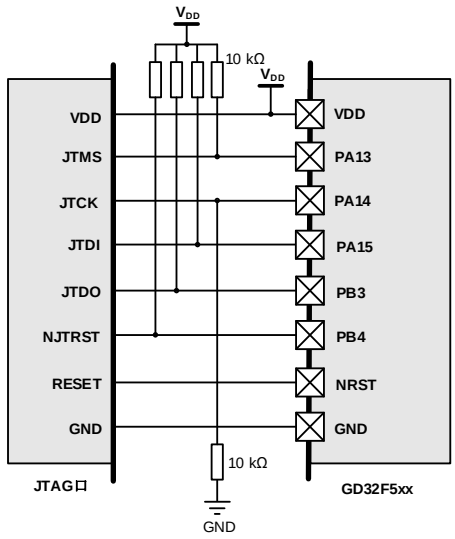
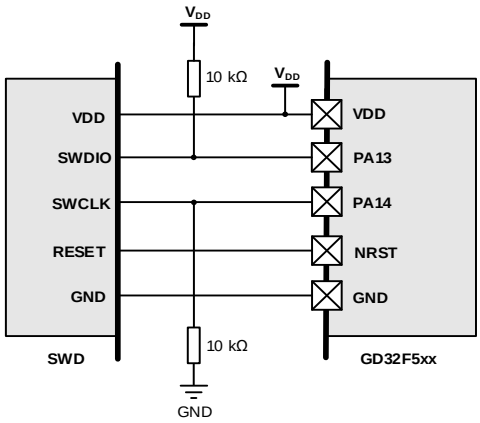


Table 2-15. Allocation of SWD download debug interfaces

Alternate function	GPIO port
SWDIO	PA13
SWCLK	PA14

Figure 2-41. Recommended SWD wiring reference design

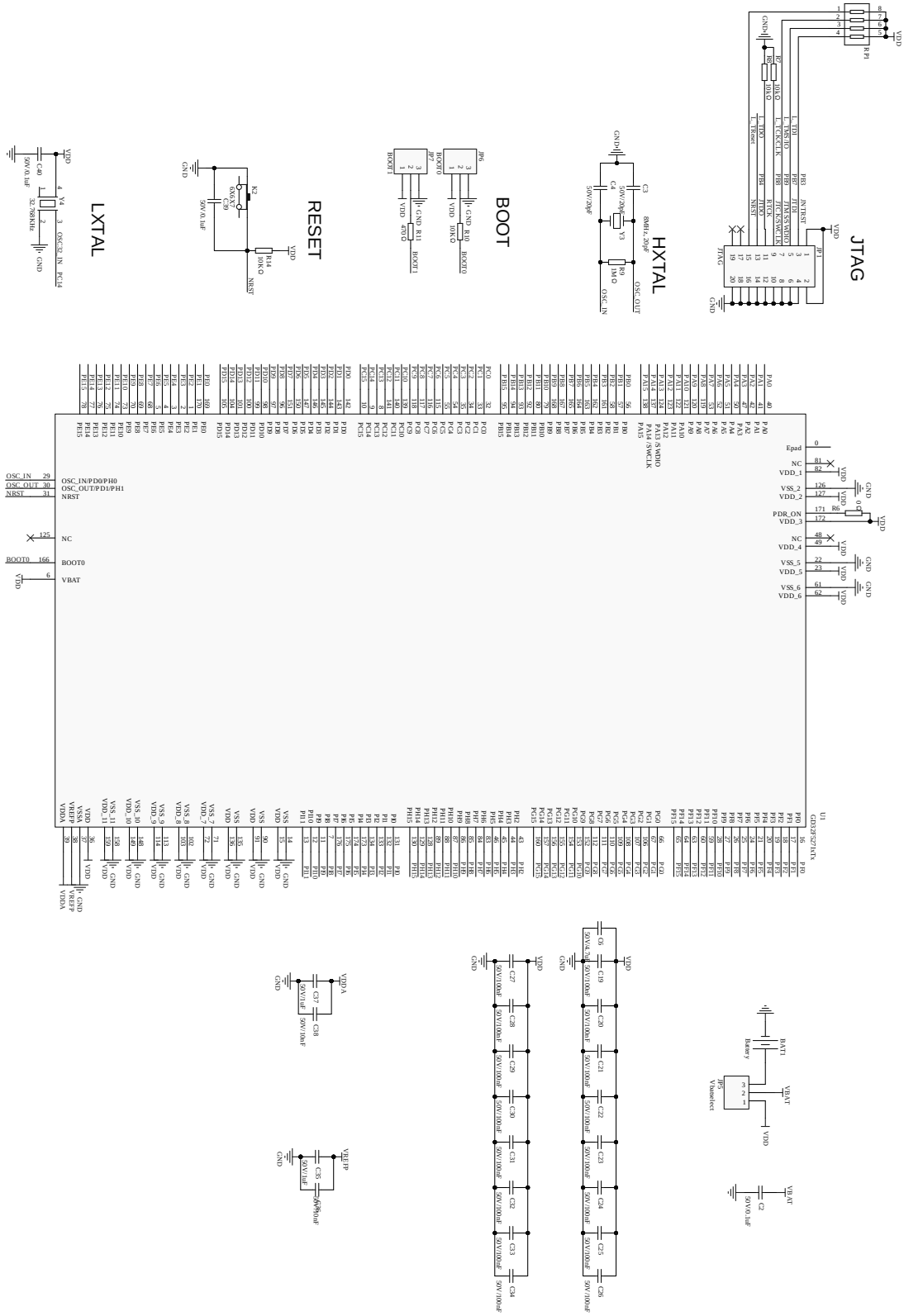


The following methods can be used to improve the reliability of SWD download debug communication and enhance the anti-interference capacity of download debug.

1. Shorten the length of the two signal wires of SWD to not more than 15 cm.
2. Twist the two SWD wires and the GND wire together.
3. Connect a small capacitor of tens of pF in parallel at two signal wires of SWD to GND.
4. Connect 100 Ω to 1 kΩ resistor to any IO of the two signal lines of SWD.

2.7. Reference schematic diagram design

Figure 2-42. Reference schematic diagram design recommended for GD32F5xx



3. PCB Layout design

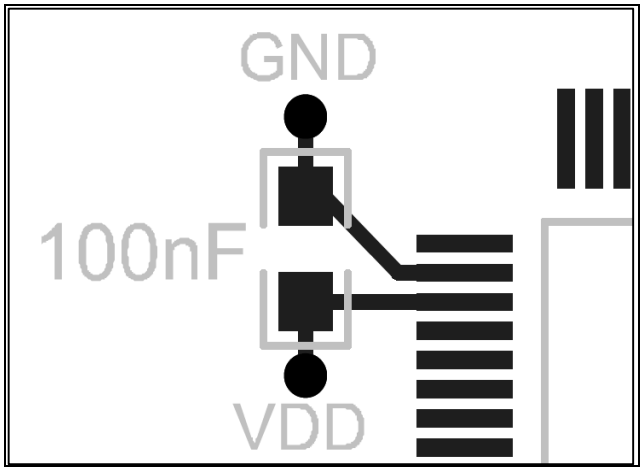
Both the performance of supporting peripheral components and the PCB layout are crucial for more stable functions and better EMC performance of MCU. In addition, if conditions permit, try to choose a PCB design scheme with an independent GND layer and an independent power layer, thus providing better EMC performance. Otherwise, it is also necessary to ensure a good power supply and grounding design, for example, by keeping the integrity of the GND plane under MCU whenever possible.

In applications with high power or strong interference, it is necessary to consider keeping MCU away from these strong interference sources.

3.1. Power supply decoupling capacitor

The power supply of GD32F5xx has V_{DD}, V_{DDA}, V_{REFP}, and other power supply pins. The 100 nF decoupling capacitor can be ceramic MLCC and must be installed as close as possible to the power supply pins. The power supply shall be wired to the power supply pins of MCU through the capacitor. It is recommended to punch vias close to the capacitor pad for the layout.

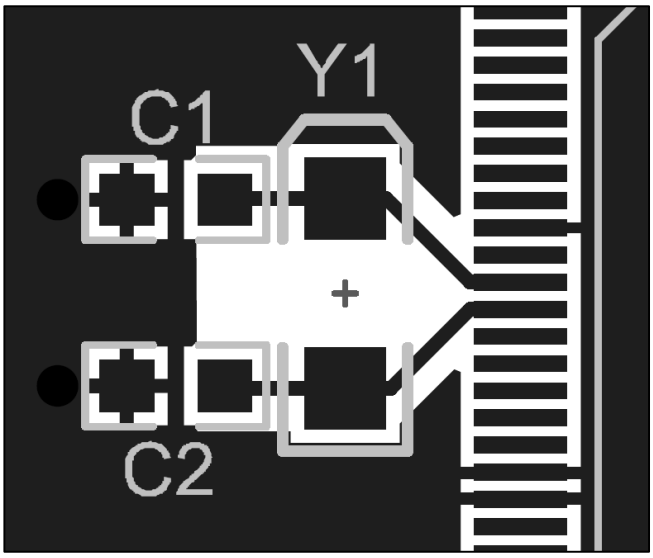
Figure 3-1. Recommended layout design of decoupling capacitor at power supply pins



3.2. Clock circuit

The clock of GD32F5xx includes HXTAL and LXTAL. The clock circuit (including the crystal or crystal oscillator and capacitors) shall be installed close to the clock pins of MCU, and the clock wiring shall be wrapped by GND as much as possible.

Figure 3-2. Recommended clock pin layout design (passive crystal)



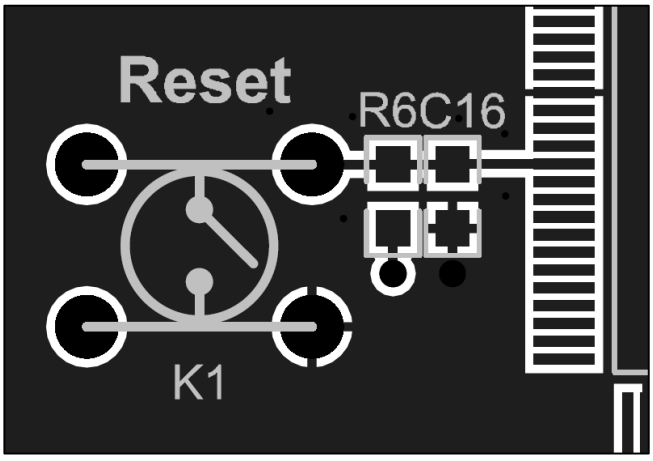
Notes:

1. The crystal shall be installed as close as possible to the clock pins of MCU, and the matching capacitors shall be installed as close as possible to the crystal.
2. The whole circuit should be arranged on the same layer as MCU as much as possible, and the wiring should not pass through the layer as much as possible.
3. Clock devices and adjacent layers below the wiring area shall be kept empty whenever possible and free of any clock-irrelevant wiring and copper laying.
4. Components with high power and strong interference risks and high-speed wiring should be kept away from the clock crystal circuit as much as possible;
5. The clock wire shall be wrapped by GND to achieve a shielding effect.

3.3. Reset circuit

The reference PCB layout for NRST pin wiring is as follows:

Figure 3-3. Recommended Layout design for NRST pin wiring



Note: The resistors and capacitors of the reset circuit should be installed as close as possible

to the NRST pins of MCU, and the NRST wiring should be kept away from components with strong interference risks and high-speed wiring as much as possible. If conditions permit, it is better to wrap the NRST wiring by GND to achieve a better shielding effect.

3.4. USB circuit

For GD32F5xx MCU, the USBFS module has two differential signal lines (namely DM and DP). After the USBHS module is connected to the external high-speed PHY, two differential signal lines (namely DM and DP) will also be led out in the PHY chip. It is recommended to apply 90 Ω characteristic impedance to the PCB layout and wire the differential signal lines to a minimum length whenever possible in strict accordance with the equal length and distance rule. If the two lines are unequal in length, the shorter line can be compensated for with a snake-shaped line at the end. Considering impedance matching, about 50 Ω series matching resistor is recommended.

The reference wiring of the differential signal lines (DM and DP) is as follows:

Figure 3-4. Recommended layout design for wiring of differential signal lines (DM and DP) (1)

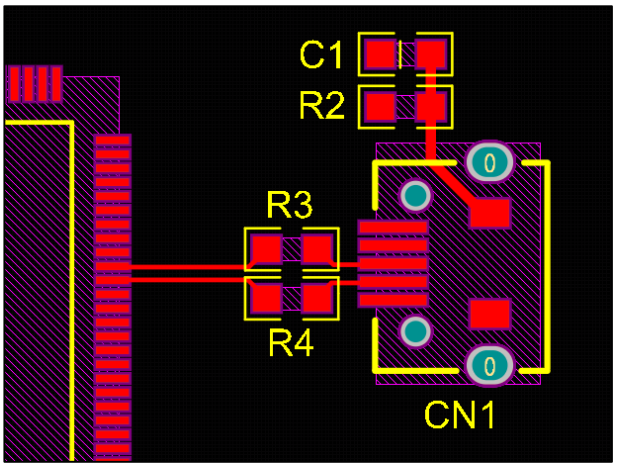
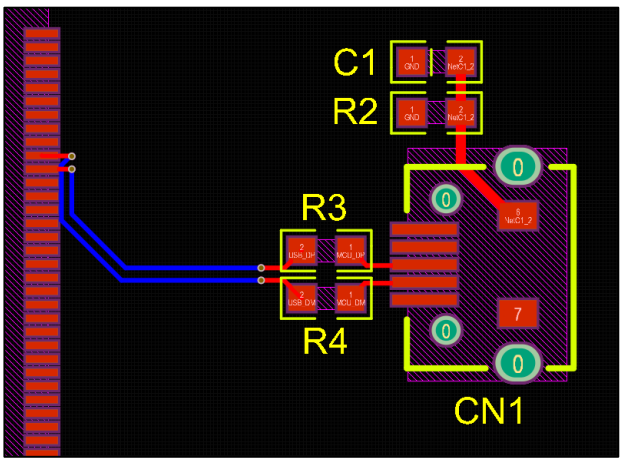


Figure 3-5. Recommended layout design for wiring of differential signal lines (DM and DP) (2)



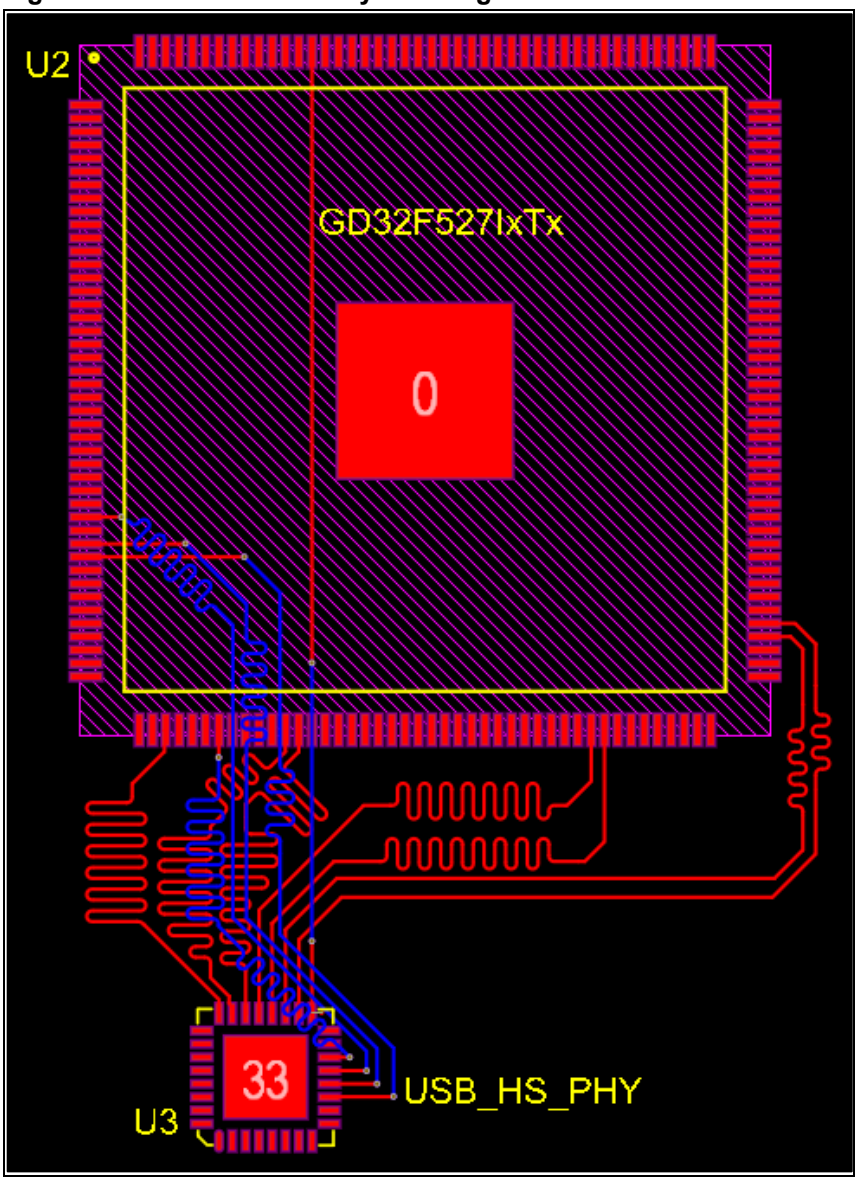
Recommendation: R3 = R4 = 50 Ω, R2 = 1 MΩ, C1 = 4700 pF.

Notes:

1. Provide a proper layout to shorten the wiring distance of the differential signal lines.
2. Draw two differential signal lines first, on which there shall be up to two pairs of vias in symmetrical layout.
3. Wire two lines in symmetrical and parallel manner for close coupling. Avoid arced, 45° or 90° wiring.
4. Symmetrically arrange the resistance-capacitance and EMC devices connected to the differential signal lines or test points thereon.

For the USBHS module, the data line and signal control line between MCU and external HS PHY shall be wired as short as possible to the same length with the snake-shaped line. See the following figure for reference:

Figure 3-6 Recommended layout design for MCU and PHY



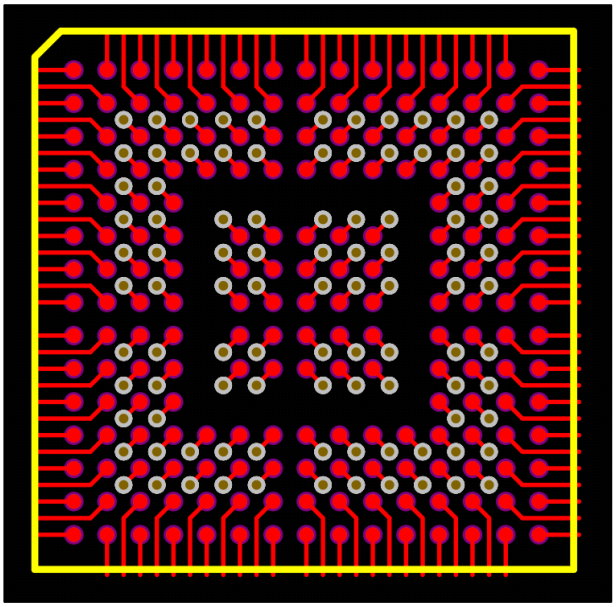
Notes:

1. Only the lines between MCU and USB HS-PHY are drawn in the figure.
2. A proper layout is provided for as compact space as possible between the USB HS-PHY chip and MCU.
3. The longest signal line is set as the target during layout, while other signal lines are compensated for with snake-shaped line.

3.5. Fan-out of BGA package

Some models of GD32F5xx MCU have BGA176(0.65 mm Pitch) package, for which the following wiring rules and fan-out modes are recommended.

Figure 3-7. Fan-out mode of BGA176 package



For BGA (0.65 mm Pitch) package, the wiring diameter of a single pin is not recommended to be larger than the pad diameter, namely 0.25 mm. It is recommended to set 4 mil line width and space according to rules and fan out by using 8/12 mil (in case of large passing current, 8/13 mil is acceptable; however if 8/13 mil is exceeded, 4 mil line width and space can not be led out) via, as shown in ***Figure 3-7. Fan-out mode of BGA176 package***. The via-pad distance is 6.2 mil.

4. Steel mesh and soldering

4.1. Steel mesh

When SMT is applied, the thickness and opening size of the leak of the steel mesh depend on the type of solder paste and the distribution, density, and spacing of pad openings. Overlarge opening of the leak of the steel mesh often leads to distribution of too much solder paste, which is prone to "bridging" during soldering. Too small opening of the leak will lead to application of little solder paste and thus cause insufficient strength of the solder joint or "cold solder".

4.1.1. Recommended thickness of steel mesh

The thickness and opening size of the steel mesh generally follow these rules: The width-to-thickness ratio shall be higher than 1.5 (that is, the opening width of the steel mesh shall be 1.5 times the thickness of the steel mesh or above), and the area ratio shall be higher than 0.66 (that is, the opening area of the steel mesh shall be 0.66 times the lateral area of the opening column or above), which can ensure to the greatest extent that there is proper amount of solder paste on the pad when brushing.

The recommended thickness of the steel mesh of GD32F5xx new products are listed in ***Table 4-1. Recommended thickness of steel mesh of GD32F5xx chip***.

Table 4-1. Recommended thickness of steel mesh of GD32F5xx chip

Chip package	Thickness (mm)
LQFP176(24x24, 0.5pitch)	0.12
BGA176(10x10, 0.65pitch)	0.12
LQFP144(20x20, 0.5pitch)	0.12
LQFP100(14x14, 0.5pitch)	0.12
LQFP64(10x10, 0.5pitch)	0.12

In practice, the above table can only be for reference for the thickness of the steel mesh of GD32F5xx products. The thickness of the steel mesh of PCB shall be evaluated in combination with the density of PCB devices, pitch value of other chip pins, pad dimensions, and process requirements.

4.1.2. Cleaning and use of steel mesh

Cleaning

- The steel mesh shall be cleaned before use to remove contaminants contacted during transportation or long-term storage.
- The steel mesh shall be cleaned in time after use and packed in a special storage position.
- The steel mesh to be cleaned shall not be placed randomly to prevent it from being

damaged or bringing other contaminants.

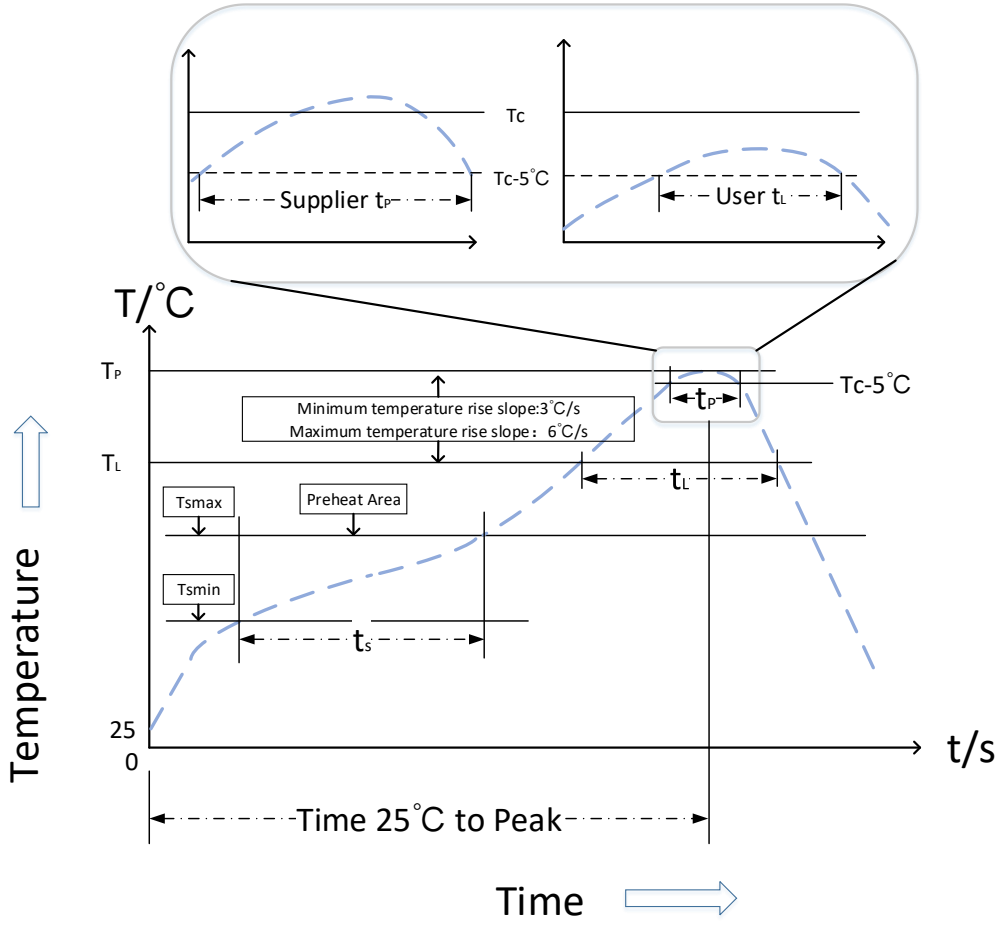
- The steel mesh shall be placed vertically in a special storage position and isolated from each other.

Use

- Solder paste for soldering shall be applied after being heated and stirred evenly to prevent the steel mesh from being blocked.
- The steel mesh shall be gently moved to prevent bumping against hard objects or sharp devices.
- When brushing, the steel mesh shall be kept close to PCB, and attention shall be paid to the adjustment of the pressure on the scraper until there is no residual solder paste on the intact steel mesh.
- The steel mesh shall be lifted for demolding at a proper speed about 3 s after brushing.
- When reaching the service life limit, generally 100,000 times, the steel mesh shall be scrapped.

4.2. Soldering

Figure 4-1. Recommended reflow soldering temperature curve



During actual processing and production, the reflow soldering temperature curve shall be set

with reference to many factors, including component characteristics, PCB material, component distribution density, and solder paste composition. The above soldering temperature curve for GD32F5xx chips is introduced below for reference.

Table 4-2. Reflow soldering parameters

Characteristic parameter	Lead-free assembly
Average temperature rise slope from 217 °C to peak temperature	Maximum 3 °C / s
Preheating duration (150 °C to 200 °C)	60 s to 120 s
Duration for keeping the temperature above 217 °C	60 s to 150 s
Peak temperature	260 + 5 / - 0 °C
Duration for true peak temperature of below 5 °C	30 s
Temperature drop slope	Maximum 6 °C / s
Duration for temperature rising from 25 °C to peak temperature	Maximum 8 min

5. Package description

GD32F5xx has a total of five package types, namely BGA176, LQFP176, LQFP144, LQFP100, and LQFP64.

Table 5-1. Description of package types

Product model	Package
GD32F527IxK6	BGA176(10x10, 0.65pitch)
GD32F527IxTx	LQFP176(24x24, 0.5pitch)
GD32F527ZxT6	LQFP144(20x20, 0.5pitch)
GD32F527VxT6	LQFP100(14x14, 0.5pitch)
GD32F527RxT6	LQFP64(10x10, 0.5pitch)

(dimensions in mm)

6. Revision history

Table 6-1. Revision history

Revision No.	Description	Date
1.0	Initial release	Dec. 20, 2023
1.1	1.Refine the content related to power supply detection and reset, and add Section 2.2. 2.Modify Recommended circuit design for PDR_ON pin。 3.Modify the description of the power supply method for the VREFP pin in the power supply design.	Dec. 15, 2024

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